SiC STATIC INDUCTION TRANSISTORS

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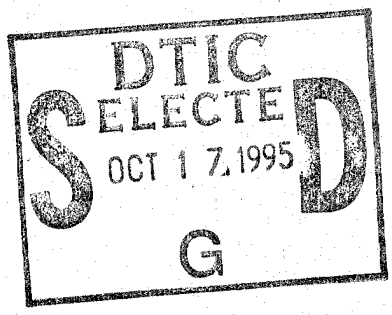
SiC Electronics

January 25, 1995

Final Report
Office of Naval Research
Contract No. N00014-92-C-0129



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FOREWORD

This is the final report on the program "SiC Static Induction Transistors" conducted by a team of scientists at the Westinghouse Science & Technology Center, Pittsburgh, PA for the Office of Naval Research during the period from August 1, 1992 to September 30, 1994. The program technical monitor was Dr. Y. S. Park of ONR. The Westinghouse co-principal investigators were R. C. Clarke, Fellow Engineer and Dr. C. D. Brandt, Mgr., SiC Device Development. Dr. Richard H. Hopkins, Mgr., SiC Electronics had overall responsibility for the project.

Major strides in the development of SiC static induction transistors (SITs) were made including (1) fabrication for the first time of operating devices at microwave frequencies, (2) demonstration of power densities of 20w per centimeter source periphery with 50% power added efficiency, (3) operation of devices with cutoff frequency to 5 GHz, and (4) model analyses which confirm the significant power will be available from SiC SITs at S-band frequencies.

ABSTRACT

SiC recessed gate static induction transistors (SITs) have been demonstrated for the first time. These early devices exhibit three times the power density of comparable silicon bipolar microwave devices at frequencies up to 500 MHz and exhibit efficient operation and high breakdown voltages. Key device fabrication processes developed in this program including reactive ion etching, Schottky gate metallizations, gate-source insulators and sharp epitaxial layer profiles.

1. SUMMARY

The results of the program provide a significant advance in the state-of-the-art for silicon carbide (SiC) microwave power devices: the demonstration of the world's first SiC static induction transistors (SITs). This is the first step in the development of high power microwave devices needed for future low-cost, compact ship and airborne radar and communications systems.

The first recessed gate SITs, fabricated using Westinghouse 4H wafer and epilayer technology demonstrate several key features required for scale-up to high power:

- Classic triode-like I-V characteristics.
- Power density three times that of silicon bipolar microwave devices.
- 12 w/cm power and 60% power-added efficiency at 500 MHz.
- High voltage operation was achieved (240V).
- F_{max} values to 5 GHz with 6 dB small signal gain at 2 GHz.
- DC device yields up to 50% on some chips.

In addition to these performance demonstrations, advanced reactive ion etching methods were developed to enable gate recessing, a Pt gate Schottky structure was devised, and CVD oxides were developed to insulate gates and sources. Substrate resistivities to 0.009 ohm-cm were achieved and epilayers with both sharp doping profiles and a wide doping range (10^{14} to 10^{19} atoms cm^{-3}) were produced. Two dimensional, physically-based models were developed and employed to define SIT feature sizes, epitaxial profiles, and to facilitate current and voltage tradeoff studies in the design of these early devices.

2. INTRODUCTION

2.1 NAVY SYSTEMS NEEDS FOR HIGH POWER TRANSISTORS

Present and planned U. S. Navy radar systems have a pressing need for higher power, lighter weight, more reliable equipment. The Navy has been very successful in implementing solid-state replacements for tube transmitters toward these ends. These efforts have greatly enhanced reliability and improved performance in several critical areas, such as bandwidth, stability, and maintainability. A significant limitation in the state of the art for solid-state transmitters is the power level of the transistors. The transistors are the building blocks for the transmitter, and the size, weight, and cost of the transmitter are directly proportional to the number of transistors used. Higher power transistors would translate directly to fewer power amplifier modules, lighter weight, and lower cost.

Such transistors made from SiC could make practical the production of solid-state transmitters, for systems such as upgrades to the AN/APS125/135/145 family of UHF radars on the E-2 airborne early warning (AEW) system, and the upgrade of the S-band transmitter for the AN/SPY-1 radar on the AEGIS-class ships. In each case SiC transistors, with only a modest factor of two to four increase in power density over that of silicon technology, would actually allow the transmitter volume and weight to be reduced by as much as 20% to 50%.

Our analyses outlined in Section 2.3 indicate the SiC Static Induction Transistor (SIT) is ideally suited to meet these system needs.

2.2 PROGRAM GOALS

The overall goal of this program is to develop SiC semiconductor material and device processing and to fabricate SiC static induction transistors with significantly

greater (up to 4X) the power density of silicon or GaAs microwave power transistors; specific technical objectives included:

- Develop discrete SiC SITs exhibiting up to 10w continuous power and transistors with up to 160w at S-band frequencies.
- Produce low resistivity 6H SiC substrates with a goal of 0.007 ohm-cm.
- Develop epitaxial SiC structures suitable for SIT operation.

2.3 STATIC INDUCTION TRANSISTORS AND THE SIC SIT

This discussion describes the operating characteristics of the Static Induction Transistor (SIT), compares it with those of the microwave MEtal Schottky Field-Effect Transistor (MESFET), and clearly illustrates the superior power capability of the SIT. SIT devices have higher power per unit periphery, smaller physical size, and demonstrate higher voltage operation at higher impedance levels than do MESFET devices. It is for these reasons that, when combined with the advantageous materials properties of SiC, the SiC SIT should exceed the power generation performance of the silicon SIT, the SiC MESFET, and the GaAs MESFET for hybrid applications from VHF through S-band.

The static induction transistor (SIT) invented by Watanabe and Nishizawa[1] in 1950 had a multichannel structure; it controlled current flow by means of the static induction or electrostatic field surrounding two opposed gates. Many years passed before transistor fabrication technology was sufficiently developed to take advantage of this concept. In 1975, however, experimental SITs were fabricated[2] and the source-drain current of this device was shown to follow the predicted space-charge injection model. Between 1975 and 1982 a number of articles on the subject were published in Japan and in the United States by Japanese researchers.[1-13] More recently, due to some early successes in demonstrating very high-power performance and very broad-band performance,[15-24] SIT technology has received increased attention in the United States.

2.3.1 SIT Operation

SITs are a class of transistors with a short-channel FET structure in which a current flowing vertically between source and drain is controlled by the height of an

electrostatically induced potential energy barrier under the source. This electrostatic barrier develops at pinch-off when negatively charged opposing gate depletion layers coalesce to completely deplete the source-drain channel of mobile charge carriers. Analogous to the vacuum triode, both the gate (grid) voltage and the drain (anode) voltage affect the drain (anode) current because, in the SIT, the height of the induced electrostatic barrier is influenced by both these potentials. Figure 2.1 is a two-dimensional drawing of a fundamental SIT cell where the mobile charge density is indicated by means of contours. The potential barrier from source to gate can be visualized by plotting the potential under the gates as a function of distance between the source and drain, as in Figure 2.2. If the drain potential is increased to VD2, the barrier height reduces as shown, and more current will flow in the drain circuit. Because the SIT channel is fully depleted, a change in the drain potential generates a current change even if the gate potential is not varied. Thus, the SIT has unsaturated (triode-like) current-voltage characteristics rather than the saturated (pentode) characteristics of a conventional MESFET. A set of typical SIT dc current-voltage characteristics is shown in Figure 2.3. The SIT geometry illustrated in Figure 2.1 is known as a surface-gate SIT, but several other forms of this device exist.

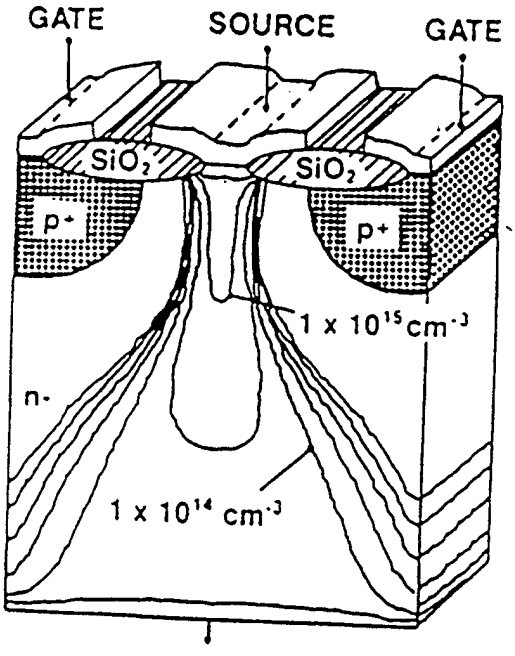


Figure 2.1 - Surface gate SIT unit cell.

The next section compares various detail functions of the SIT with the counterpart functions of a FET.

2.3.2 Advantages of SIT Devices Over MESFETs for Power Applications

1. The higher impedance and smaller physical size of the SIT leads to higher output power. To obtain high microwave power, many transistor unit cells must be combined in parallel to raise the circuit current and increase the power triangle.

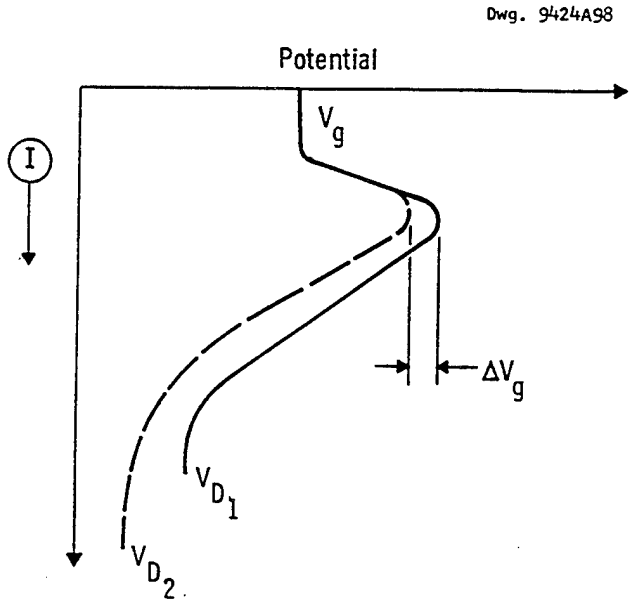


Figure 2.2 — Elementary SIT cell: potential barrier illustration.

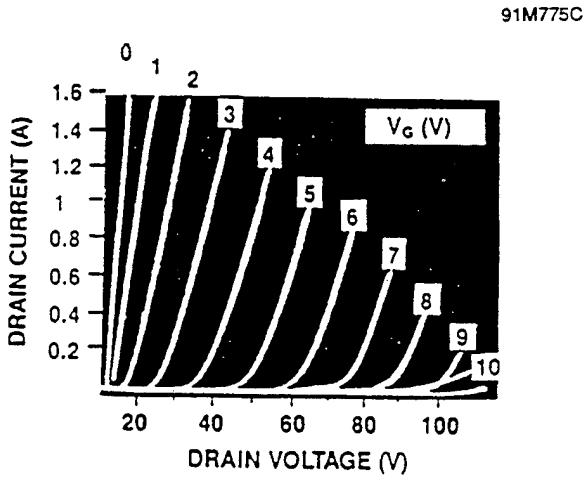


Figure 2.3 — Surface gate SIT (SGSIT) dc IV characteristics.

Since only two electrodes are needed on the surface in a SiC SIT, thus eliminating source airbridging, the unit cell area can be on the order of three to four times smaller than that of a comparable MESFET unit cell. This reduction in device size translates into four times the possible power output before phase variations in the input signal make further combining of devices ineffective.

2. SITs offer more linear amplification than MESFETs. Linearity is very important for the power devices used in radar and ECM systems to avoid unwanted harmonic generation that give an identifiable signature to the system. MESFET circuits have been difficult to realize in this regard because they suffer from an inherent nonlinearity stemming from the square law dependence of the gate capacitance on the gate voltage. This nonlinearity is not found in SIT devices because the channel is depleted of free electrons, and gate capacitance is insensitive to applied voltage. SITs therefore have very useful linear amplification characteristics.

3. Higher drain voltage and improved linearity of the SIT will give high drain efficiency. High efficiency of power conversion is critical in air and space-borne systems in order to minimize heat generation and reduce system weight and volume. SIT devices offer very high dc-to-rf conversion efficiency because of their much higher voltage and improved linearity compared to MESFETs. For these reasons, more efficient class B, C, and E transistor operation is possible with SITs than is normally available from MESFETs. For example, currently available silicon SITs show 70% drain efficiency at very high (100 W) power levels; this may be compared with GaAs power MESFETs which are limited to a few tens of watts at 30% conversion efficiency.

4. SITs are inherently less subject to the presence of surface states. SIT devices have a vertical geometry in which the gate-to-drain high-field region may be several microns below the surface of the semiconductor. This is in contrast to a MESFET, where electrons travel in a surface layer and are thus more susceptible to the disturbing influence of any oxide, surface, or interface states or charges present in the passivation layer. These defects can adversely affect the breakdown voltage and frequency response of MESFETs.

5. SITs, being bulk devices, are inherently more reliable than MESFETs. In SITs the high-field region is well below the surface of the semiconductor, and device failure due to electromigration of contact metals in high-field regions is eliminated. This advantage will be particularly significant when the higher junction temperatures available to SiC devices are fully utilized.

6. Simpler device processing of the SIT leads to higher yields. The yield of large-periphery SITs will be higher than comparable MESFET circuits because device processing is simpler; only two of the electrodes, gate and drain, are needed on the surface of the semiconductor, and transistor cell paralleling by means of the tiny airbridges that are used in MESFETs is not needed. Furthermore, submicron lithography, which is the source of many transistor defects in MESFET circuits, is not used in SIT fabrication.

7. Static induction gives lower source resistance, resulting in higher gain than a MESFET. Parasitic source resistance, which must be minimized to extract maximum gain from a transistor, is almost zero in a SIT. Source resistance in a SIT is not, for example, dominated by the resistance of the channel between source metal and gate metal as it is in a MESFET, but rather by the distance between the edge of the gate depletion layer and the highly doped source. The several-micron wide source of a SIT delivers electrons over a broad area, thus further reducing the source resistance compared to the MESFET, which has a thin, submicron edge-fed contact. As a consequence, any degradation of transconductance attributable to source resistance will be minimized, allowing the device to take full advantage of the very high saturated electron velocity of SiC.

2.3.3 The Advantages of SiC Applied to the SIT

The SIT is a high-field device and is therefore well suited to take advantage of the desirable properties of SiC such as the high saturated electron velocity and high breakdown field.

1. Frequency. SiC has twice the saturated electron velocity of silicon and hence will be capable of twice the frequency response of a silicon SIT device.

2. Breakdown Voltage and Impedance. SiC has nearly ten times the breakdown voltage of silicon and may therefore have ten times the power performance at higher impedance levels than can be obtained from silicon SITs.

3. Heat Rejection and High-Temperature Operation. SiC has 3.3 times the thermal conductivity of silicon (ten times the thermal conductivity of GaAs) and can therefore develop greater power density than a silicon device, while retaining the same surface area and "junction" temperature. Furthermore, SiC can operate with junction temperatures as high as 500°C. This permits even higher power density operation and rugged behavior for high-temperature applications.

4. Parasitics. SiC has 17% smaller dielectric constant than silicon and will therefore have less capacitive parasitics and an increase in frequency response.

5. Native Oxide. Like silicon, SiC has a native oxide which is advantageous in processing and provides a high-quality interface with the base material.

3. APPROACH

The program approach was to address through device analysis and experiment each of the key technical issues required to demonstrate the world's first operating SiC SIT device. This approach included modeling SIT operation to define initial and improved structures, development of basic processes (such as reactive ion etching) to enable device fabrication and the investigation of techniques to produce substrates and epitaxial layers with doping concentrations consistent with SIT operation.

3.1 DEVELOPMENT OF SIC SIT TECHNOLOGY

The previous section described the operation of the SIT using a surface-gate configuration as the basis for the explanation. The design utilized a doped p+ layer as the gate. Our approach was a recessed-gate design utilizing a Schottky barrier gate structure.[26] This design has the advantage of low gate-drain capacitance, and, therefore, has potentially very high-frequency operation.

Figure 3.1 is a cross section of two unit cells of the proposed Westinghouse vertical gate SiC SIT. The drain and source contact regions are separated by the pillars, and the gate metal makes a Schottky contact with the sides of the pillars. Voltage applied to the gate contacts induces a field into both sides of the pillars, constricting the conduction region and modulating the conductivity of that region.

Fabrication of the proposed SIT (Figure 3.2) consists of

- depositing an epitaxial layer of excellent quality onto an n++ SiC substrate,
- metallizing and delineating the drain contacts,
- masking and etching the trenches between the pillars,
- shadow evaporation of metal to define the gates and form the interconnects of the gates,
- interconnection of the drain contacts,
- metallizing the source contact on the back of the wafer before
- dicing and packaging.

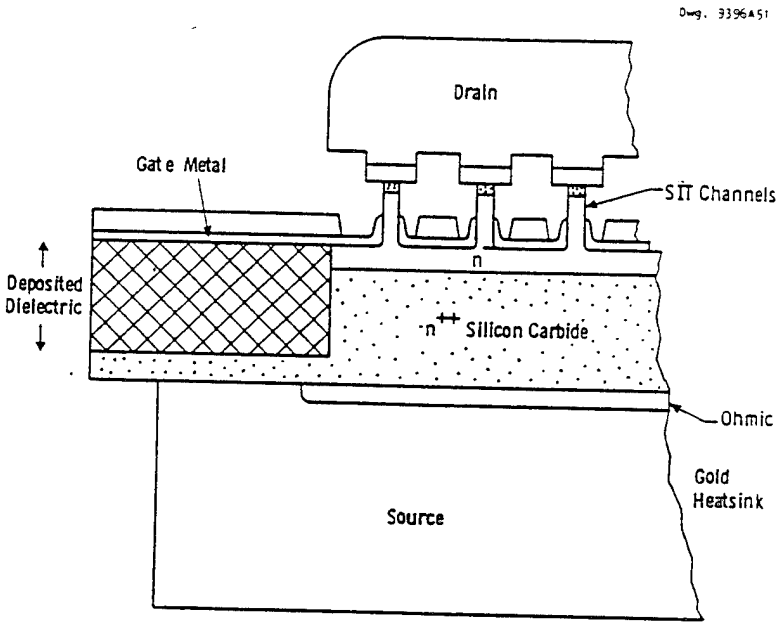


Figure 3.1 — Cross section of a recessed gate high-power microwave SiC SIT.

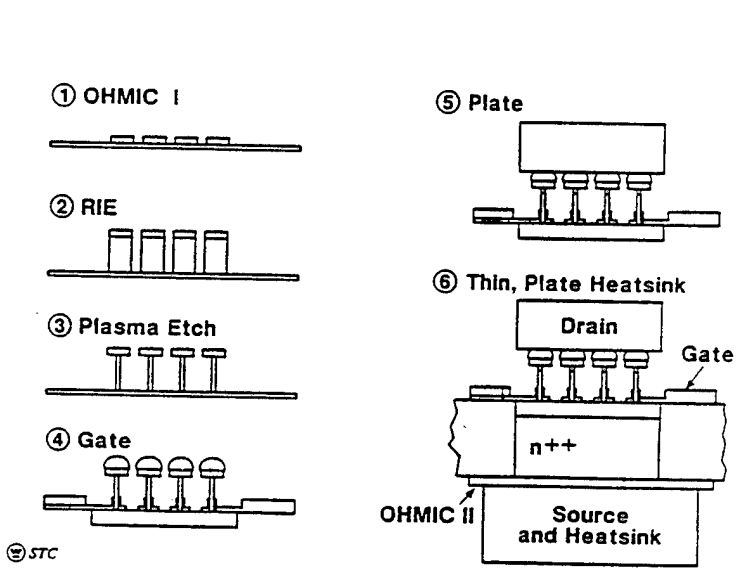


Figure 3.2 — Schematic fabrication sequence of a SiC SIT.

3.2 PROGRAM TASKS

The specific program tasks were:

Task 1 — Process Development. Investigate device fabrication processes to fabricate SIT cells with 10W of CW power. These studies include reactive ion etching (RIE), substrate thinning, surface passivation, and ohmic and Schottky contacts for operation up to 350°C. Develop schemes for combining SITs to deliver up to 160W at S-band. Mounting and packaging schemes will also be evaluated.

Task 2 — Low-Resistivity Substrates. Grow one-inch diameter 6H-SiC 0.007 ohm-cm crystals and form single-crystal wafers.

Note: When our studies showed that the election mobility of the 6H SiC polytype was too low to support the desired device performance the growth of 4H polytype boules and epilayers was successfully carried out to meet the program goals. This effort, as well as the device development, benefitted from parallel in-house material and device research.

Task 3 — Growth and Characterization of Active Layers. Evaluate CVD methods and grow active epitaxial layers with n-type dopants in the 10^{15} to 10^{19} cm^{-3} levels. Evaluate the active layers produced.

Task 4 — Modeling and Design. Model and design SITs for fabrication studies. Compare model analyses with the completed devices to verify accuracy and optimize device design.

Task 5 — Fabrication and Testing of SITs. Fabricate and test SIT cells with a goal of F_{max} of 5 GHz in the first year.

Task 6 — Device Fabrication Iteration. Fabricate a second set of devices with a goal of 10W at the end of the second year, combine devices with a goal of 160W at S-band in a 0.5 mm by 0.5 mm chip.

4. SIGNIFICANT ACCOMPLISHMENTS

This program has produced a number of significant technical achievements, including the demonstration of the first SiC SIT devices. Outlined below, task by task, are the individual accomplishments and their relationships to the original program goals. These results show the feasibility of the SIT device, the key process steps required to make it, and the basis for planning the next step in device development.

PROGRAM STATUS:

The technical outline of the program was given in Section 3. Progress on the tasks and milestones is outlined below.

TASK #1 — Process Development

The formation of current carrying pillars in SiC is essential to the fabrication of the static induction transistor. The following pillar trench process has been demonstrated:

1. An oxide layer is deposited on the SiC layered structure and densified at 1150°C.

2. A chromium-nickel mask is then defined on the oxide to act as an etch during the reactive etching of a pillar of SiC. An SEM from a wafer with this step completed is shown in Figure 4.1. *This development in processing completed the first milestone of the program.*

3. The remnant nickel mask is then removed by wet chemical etching and amorphous silicon deposited over the pillars. The amorphous silicon coats the sidewalls of the pillars planarizing the structure as shown in Figure 4.2.

4. Anisotropic reactive ion etching is then used to etch back the amorphous silicon from the field which leaves a silicon layer inside the device forming a gate structure against the sidewalls of the pillars as shown in Figure 4.3.

5. A CVD deposited oxide coat is then applied to the pillars, densified, and anisotropically etched away from the field in order to leave an oxide sidewall passivation between the source n+ SiC layer and the amorphous silicon gate electrode.

6. The amorphous silicon is selectively reactive ion etched from the wafer leaving behind an overhanging oxide structure . This overhang is then used to fabricate a metal gate on the pillar sidewall by sputtering platinum followed by dissolving the oxide in an HF based etch to lift-off excess metal. SiC pillars with attached platinum gates are shown in Figure 4.4.

TASK #2 — Produce Low Resistivity Substrates

For this program, 6H-SiC crystals with high nitrogen content were to be grown to obtain high conductivity wafers for use as substrates for epitaxial deposition of SIT device layers. SiC crystals up to 1.5-inches in diameter were grown in the c-orientation (<0001>-axis) using a modified sublimation growth system described elsewhere.[27,29] The crystals were ground and sliced into wafers. Using a diamond-based polish procedure, the substrates were then single-side polished on the Si-face. When the 4H-SiC polytype was shown to exhibit higher electron mobility without anisotropy in the c-and a-axis directions,[30] for comparison

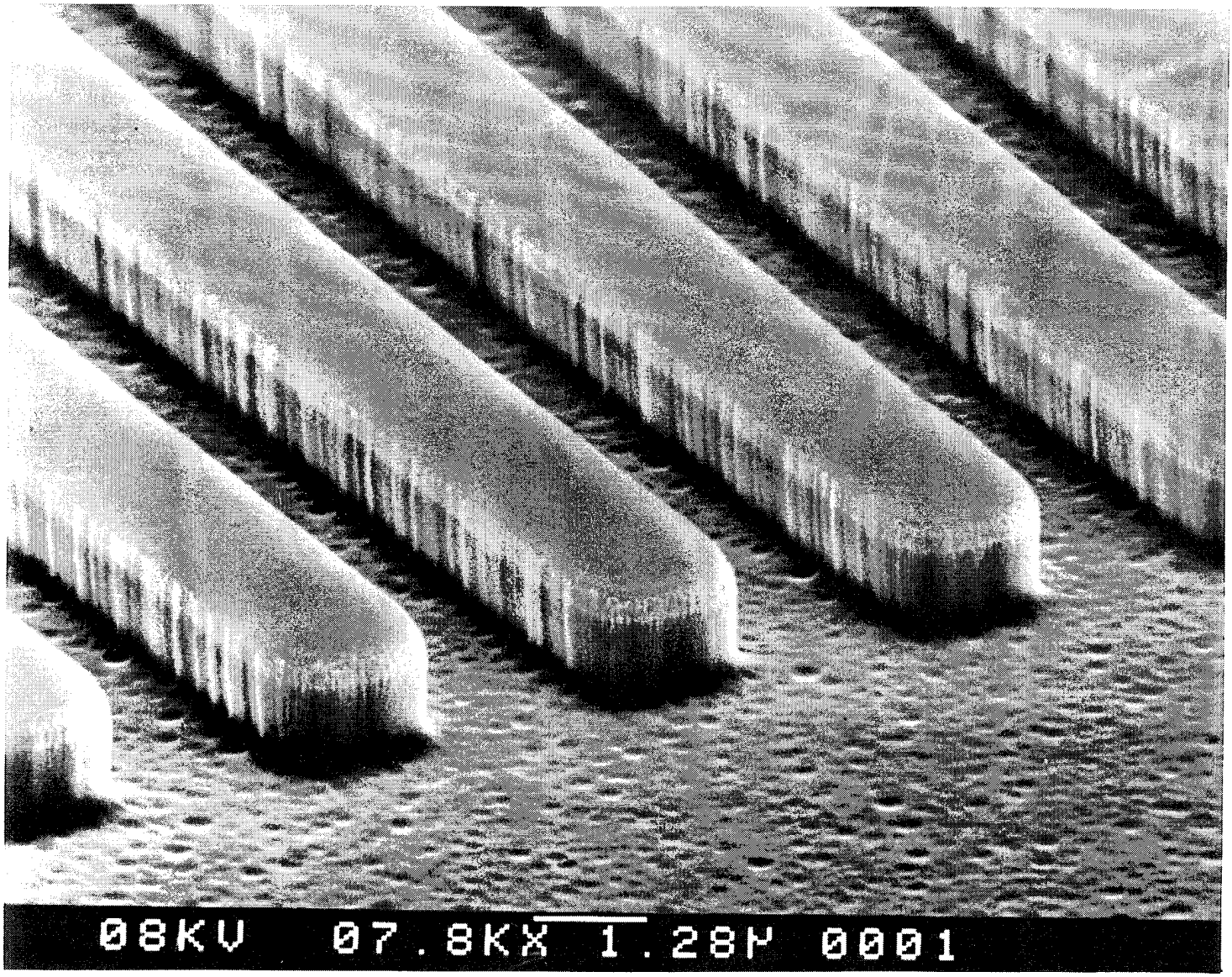


Figure 4.1 — Reactive ion etched pillars in SiC; notice the accurate definition of the pillar sidewall by the nickel mask and the clean field between pillars.

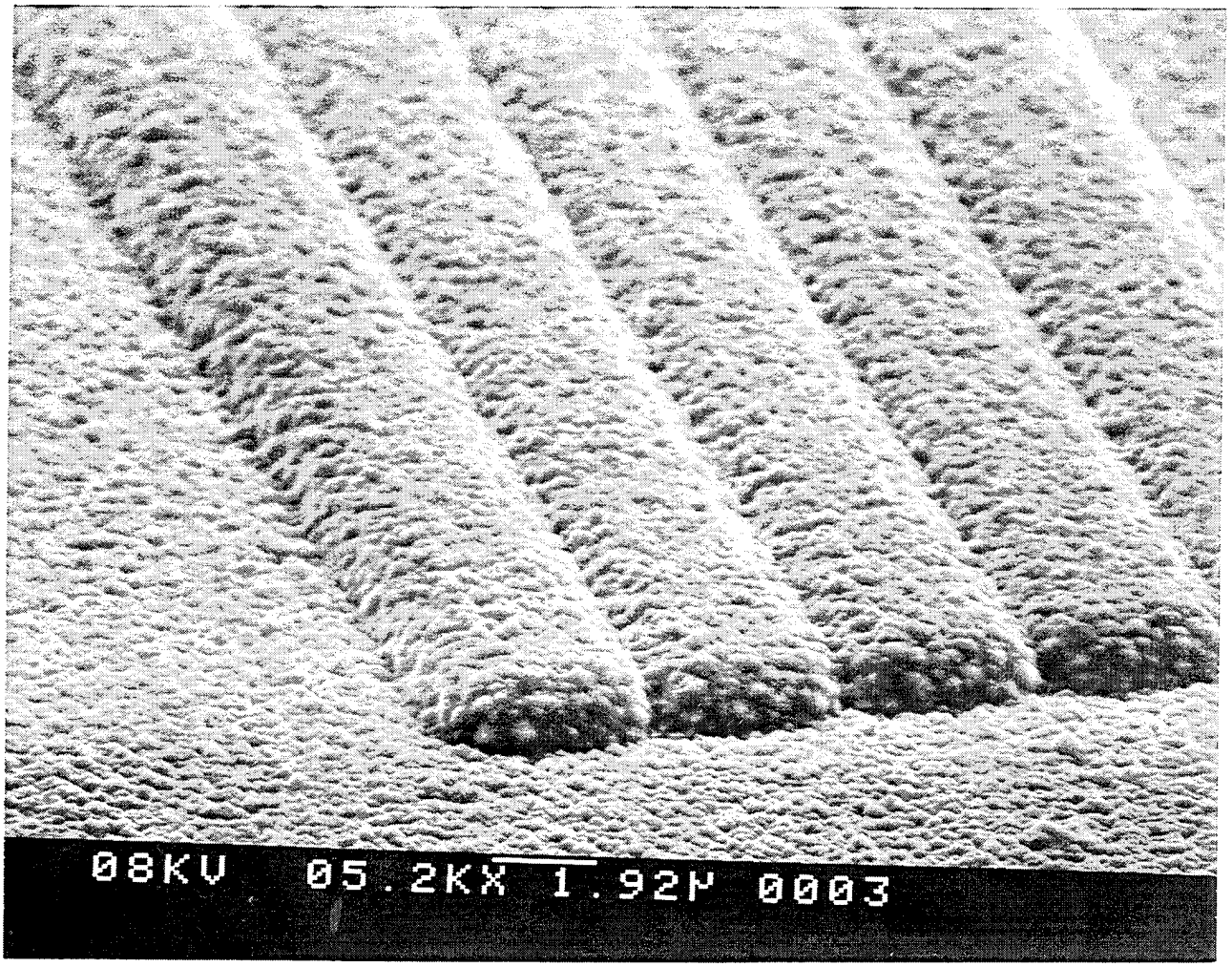


Figure 4.2 — Deposition of amorphous silicon over the pillars of Figure 4-1 planarizes the structure filling in between the pillars.

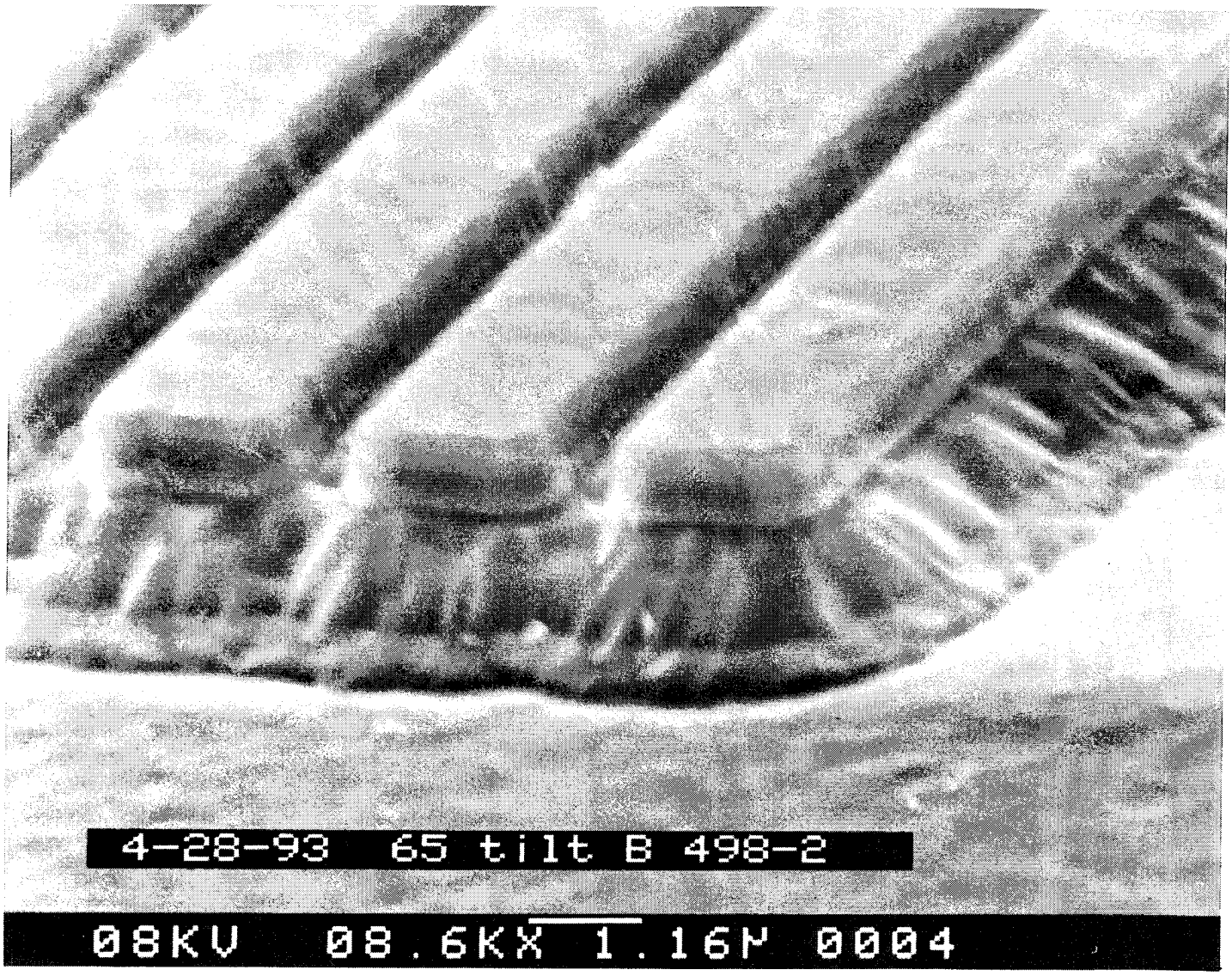


Figure 4.3 — Anisotropic reactive ion etching of the amorphous silicon removes silicon from the field between device chips but leaves a silicon gate structure between the pillars.

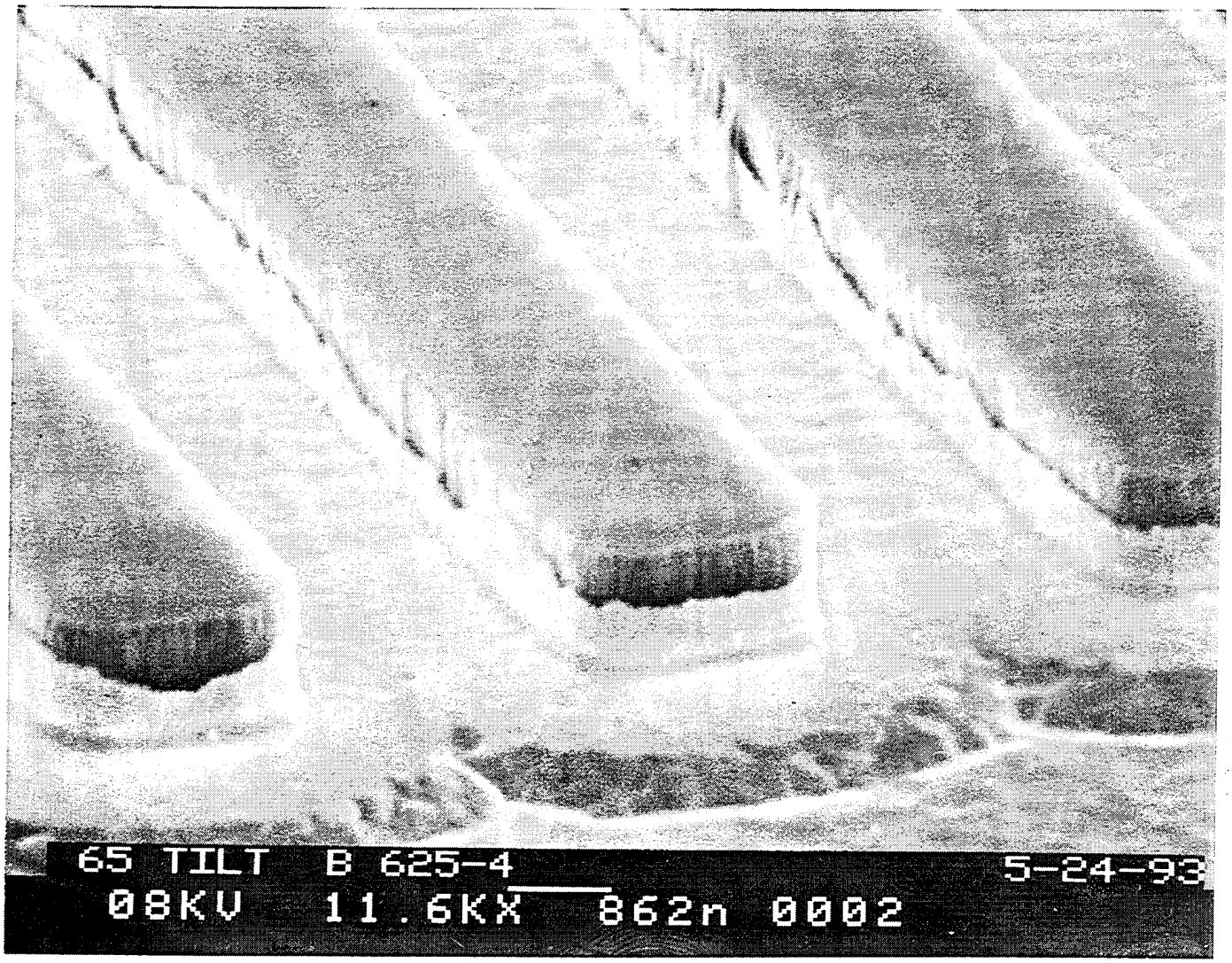


Figure 4.4 — SiC SIT pillars with attached platinum gates after removal of the oxide layer.

purposes, crystals and substrates were also prepared in the 4H- polytype, using methods developed under a separate internal Westinghouse funded program. Later in the program 4H wafers become the basis for device fabrication.

6H-and 4H- N^+ substrates were obtained by nitrogen doping during SiC sublimation growth. Figure 4.5 shows carrier concentration vs temperature data for nitrogen-doped 6H-SiC at two different doping concentrations. For the crystal with the lower doping concentration, the activation energy for the nitrogen shallow donor level derived from the slope of the curve is approximately 83 meV, consistent with that observed by other workers for nitrogen occupying the hexagonal lattice site.[30] As the nitrogen doping concentration increases, the ionization energy is observed to decrease. This reduction is exemplified by the upper curve in Figure 4.5, and has been attributed by Schoener[31] to the Pearson-Bardeen effect in which the average potential energy of the electron is reduced as the average distance between dopant atoms decreases.[32]

Figure 4.6 shows the resistivity magnitude and uniformity exhibited by 6H and 4H-SiC nitrogen-doped N^+ crystals. 4H-SiC exhibits a slightly lower resistivity owing to the reduced energy level for the nitrogen donor in the 4H lattice (approx. 45 meV). 6H substrates are typically 0.01 to 0.02 ohm-cm and 4H resistivities lie in the range 0.008 to 0.015 ohm-cm. *This result completes milestone 2.*

For epitaxial device layers exhibiting optimum layer morphology N^+ substrates with minimum defect densities [micropipes, low angle grain boundaries (LABs)] and minimal residual polishing damage (scratches, sub-surface damage) are required. The substrates utilized in these studies took advantage of improvements in both micropipe density and LABs evolved under research conducted with Westinghouse IR&D support. Near the beginning of the program, substrates exhibited average micropipe density values of >1500 cm^{-2} for a minimum resolved diameter (MRD) of >1.5 μm; correspondingly, LABs were in the 500 to

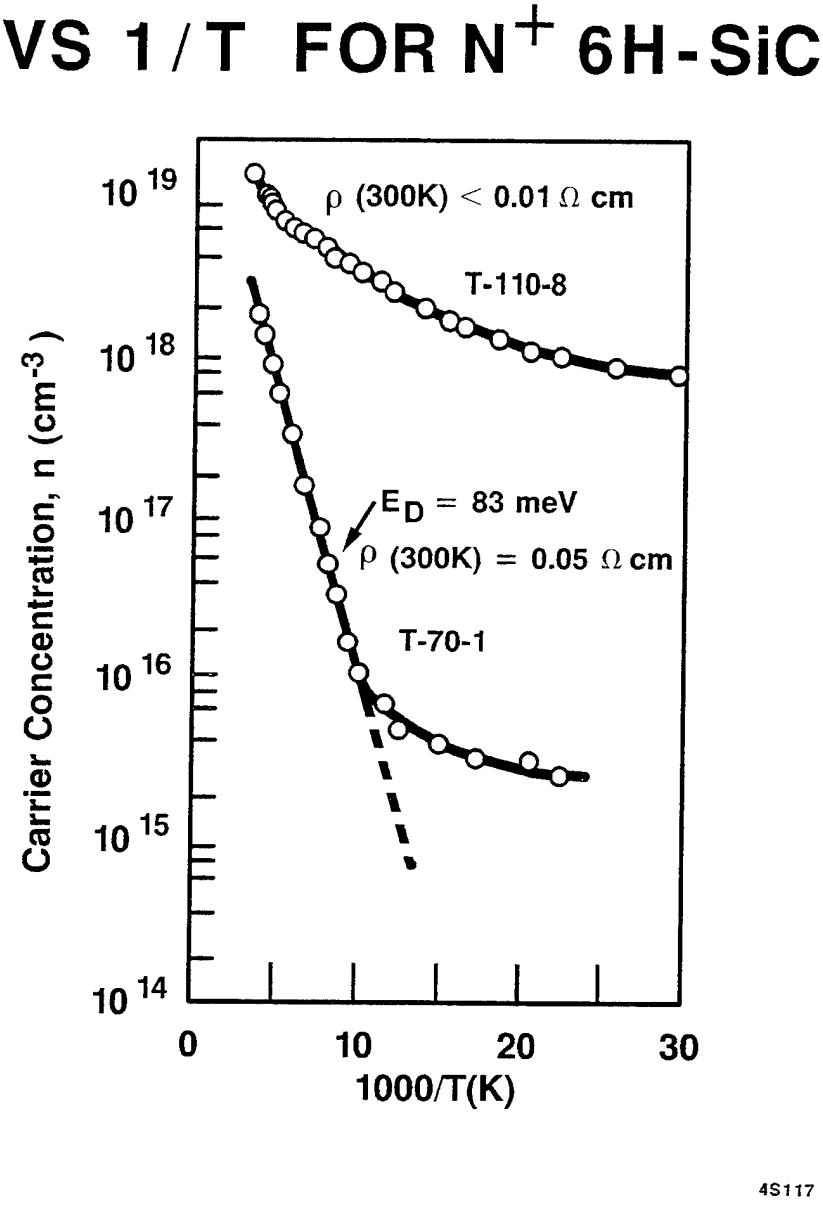


Figure 4.5 — Carrier concentration vs temperature for 6H-SiC at two different doping densities.

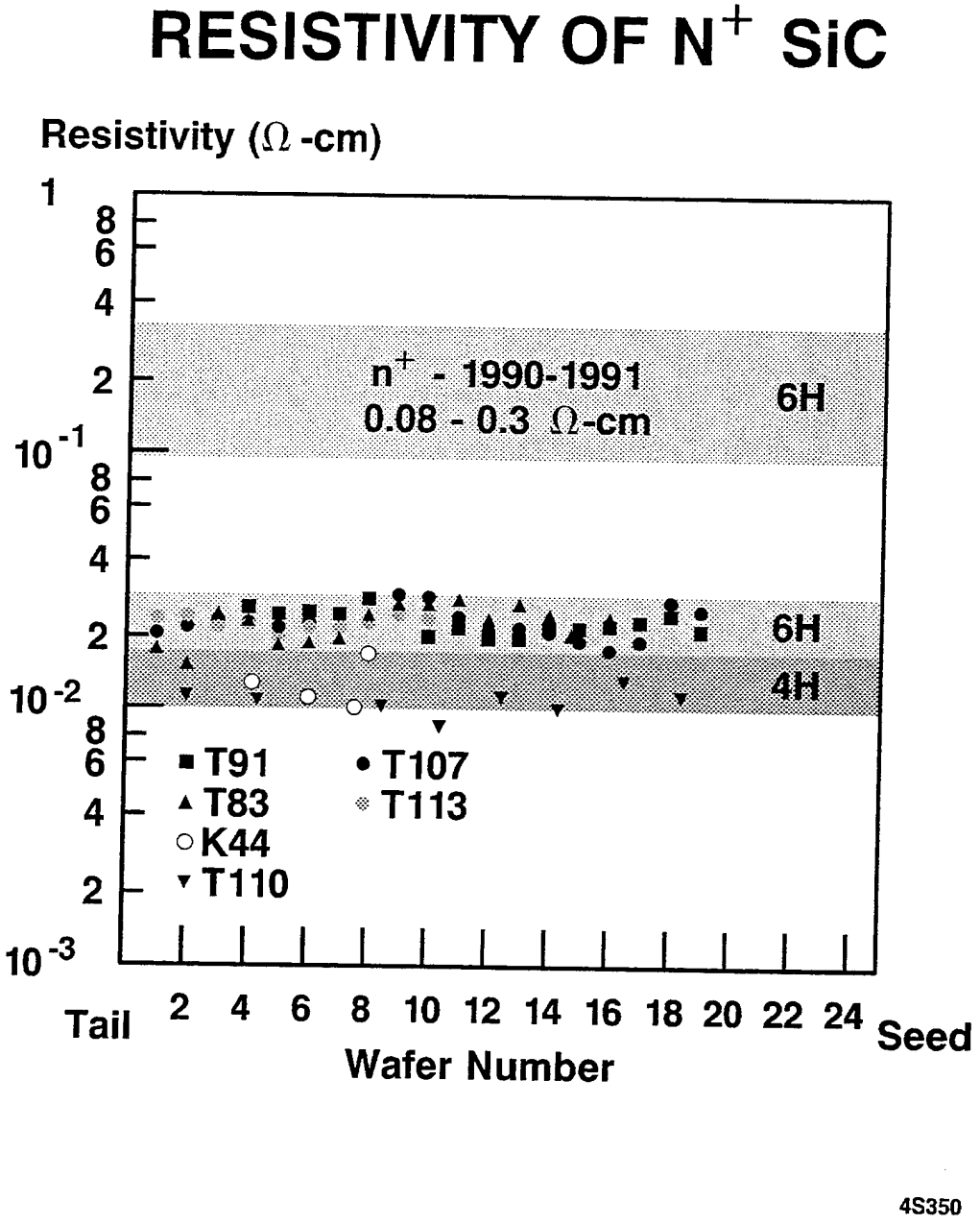


Figure 4.6 — Resistivity vs crystal length for nitrogen-doped 6H and 4H-SiC grown by the PVT method.

1500 arc-sec range. Current substrates exhibit micropipe densities in the 100 to 800 cm^{-2} range with corresponding MRD of >1 μm; and LABs approaching 100 arc-sec. Figure 4.7 shows the average macroscopic residual polish damage in current substrates, as determined by back scattering of UV light from polishing defects (scratches, etc.). The intensity of the backscattered light signal is proportional to the sub-surface damage density. Current polishing techniques developed by Westinghouse yield wafer surfaces with macro-damage defect density roughly equivalent to silicon technology.

TASK #3 — Grow and Characterize Active Layers

The static induction transistor active layer profile requires two extremes of doping, a thick 5 μm unintentionally doped buffer layer of 1 x 10^{16} cm^{-3} or below and a very highly doped >10^{19} cm^{-3}, 0.2 μm thick contact layer. To achieve the four orders of magnitude change in doping in the same profile requires precise control of growth conditions and control of nitrogen dopant.

The profile was grown using a unique, Westinghouse large capacity horizontal reactor capable of handling up to 1 – three inch diameter or three – 1.25 inch diameter SiC wafers at a time. The growth chemistry for SiC employs propane as a source of carbon and silane as a source of silicon transported via hydrogen carrier gas to an inductively heated graphite susceptor. SiC is grown homoepitaxially on c-axis orientation n-type 6H SiC substrates placed on the heated susceptor. *A SiC SIT profile developed during the program is shown in Figure 4.8. This completes the third milestone of the program.*

TASK #4 — Model and Design SIT

Two dimensional, physically based modeling has been used to predict results for SiC SITs using a commercially available device simulator from Technology Modeling Associates. We have modified the program to reflect SiC material and

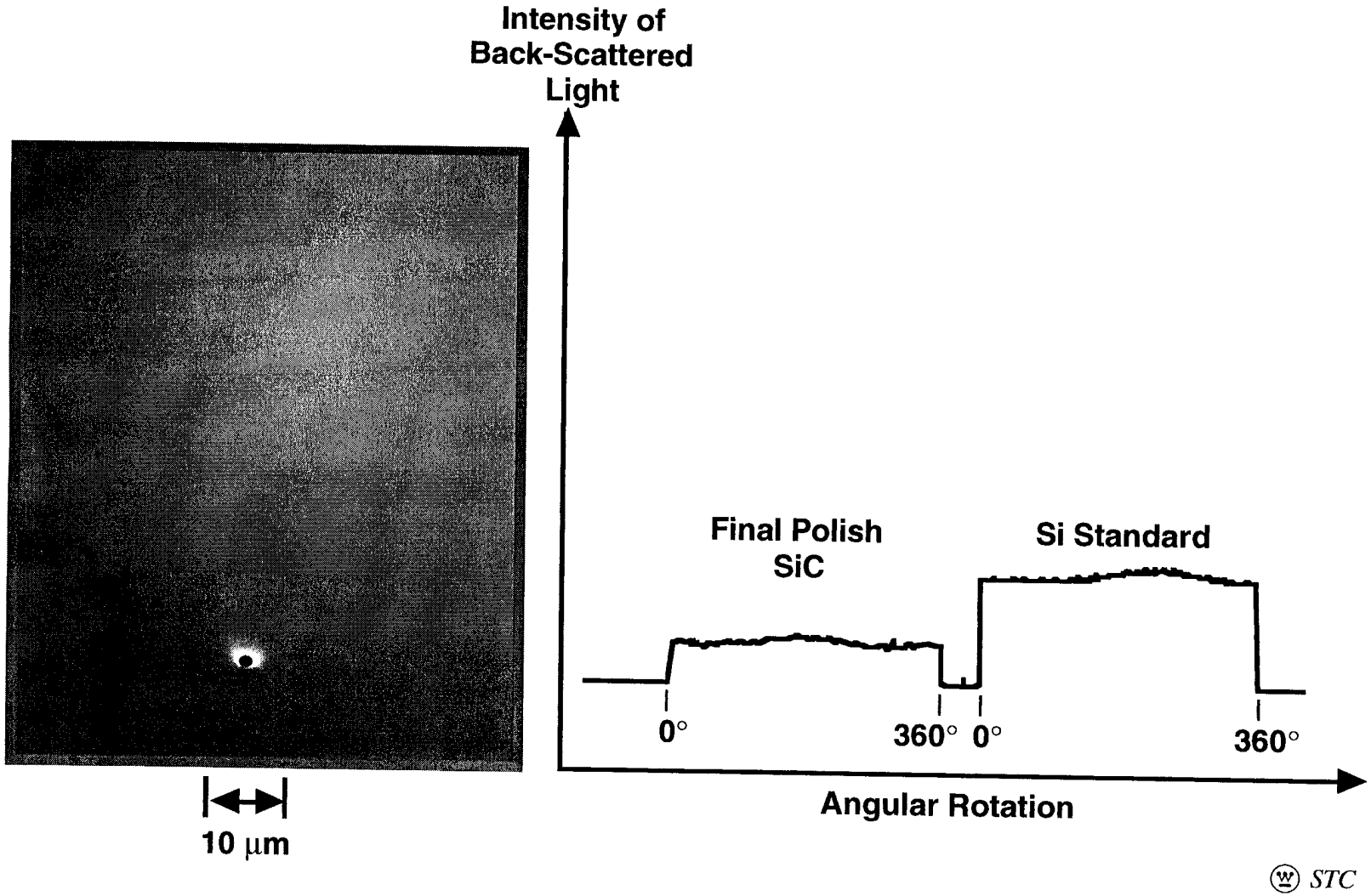


Figure 4.7 — Photograph of scratch-free surface and corresponding back scattered UV light signatures of a polished SiC substrate.

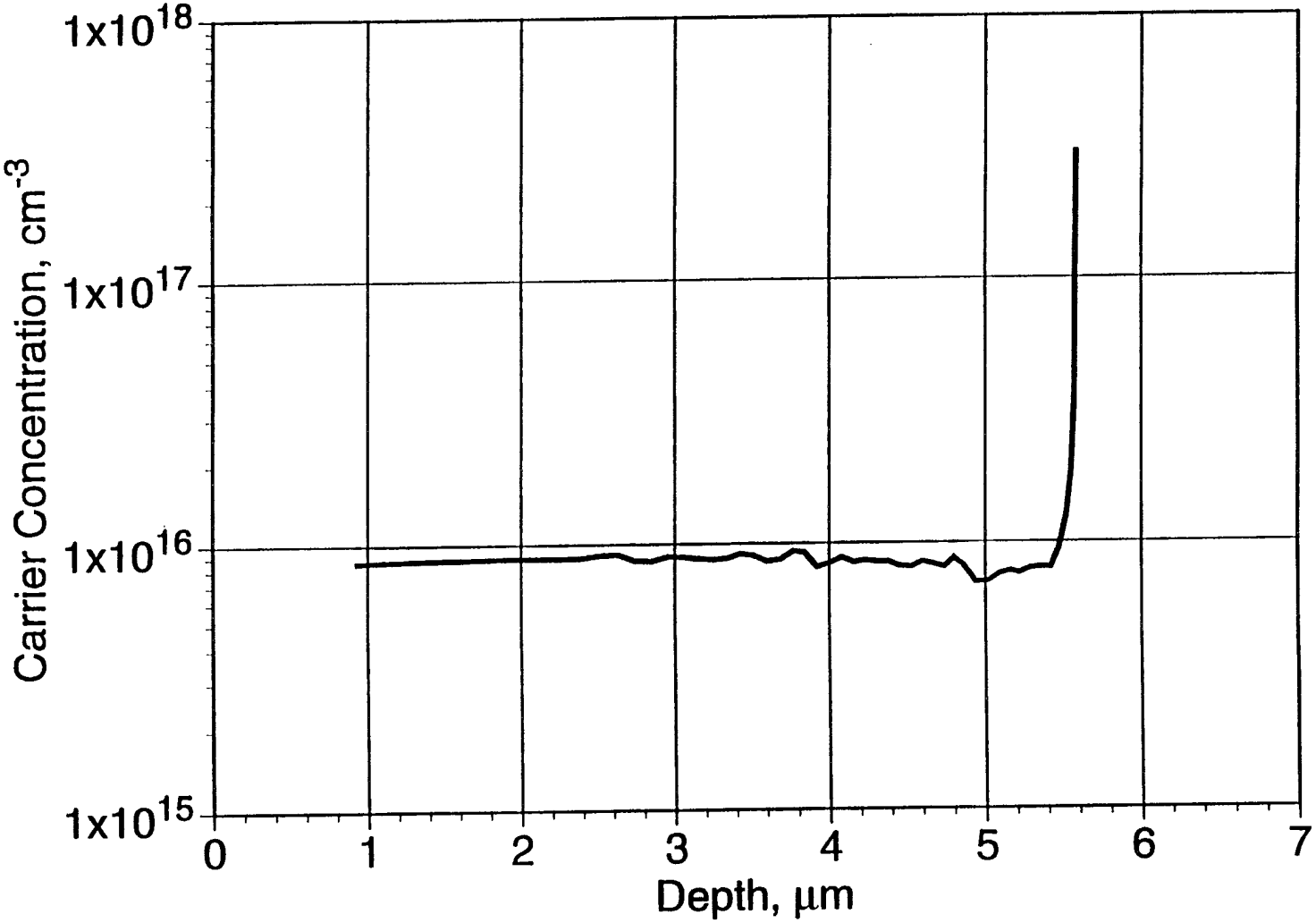


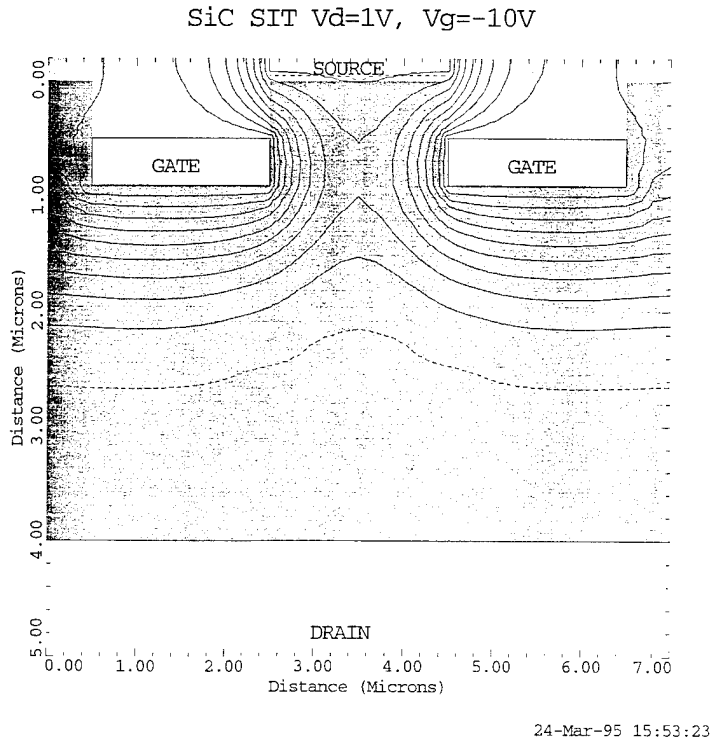
Figure 4.8 — Doping profile of a SiC SIT for transistor operation.

electrical properties and to obtain dc and small signal AC simulations. Figure 4.9 shows a cross-sectional view of the SIT in the off condition (Vd-1V, Vg=-10V). On the cross-section the constant contours of potential (solid lines) and the depletion boundary (dotted line at approximately 2.5 μm) are shown. Because the active part of the channel is fully depleted of electrons, no current flows from source to drain. In the bottom part of Figure 4.9 a three dimensional surface potential plot is shown. This potential follows the classic "saddle" nature of the potential distribution in a SIT. Evident in this figure is the potential barrier an electron sees sitting at the saddle point. Small signal predictions for this device structure indicate that 8 to 9 dB of gain is possible at 4 GHz if contact resistances can be reduced below 10^{-6} ohm cm^2 and other improvements to parasitic capacitances are made.

Figure 4.10 is analogous to Figure 4.9, with the SIT now fully turned on. From the cross sectional view, a path in the depleted region is clearly seen where electrons are being injected from the source to the drain. Using the models, a variety of design options including geometry (gate recess, spacing etc.) and epitaxial doping were explored to achieve the final and iterated mask designs for the device. Subsequently, modeling was used to refine later design iterations to meet program goals. *These results completed the requirements for Task 4.*

TASK #5 — Fabricate and Test SiC SIT

The first Schottky gated SiC SIT devices made on this program were of small source periphery, (200 μm), but showed the expected triode I-V characteristics of a SIT as shown in Figure 4.11. The device was fabricated in 6H CVD material grown on n+ substrates. A lightly doped (1×10^{16} cm^{-3}) layer forms the drift region of the device (see Figure 4.8) and an n+ cap facilitates ohmic contact formation. Referring to Figure 4.12 device fabrication was as follows: after forming the 2 μm wide SIT fingers by dry etching, ohmic contacts were sintered to the source and drain, and Schottky barrier gates were formed by lift-off of sputtered metal using an overhanging oxide structure. CVD field oxide was then applied and patterned to



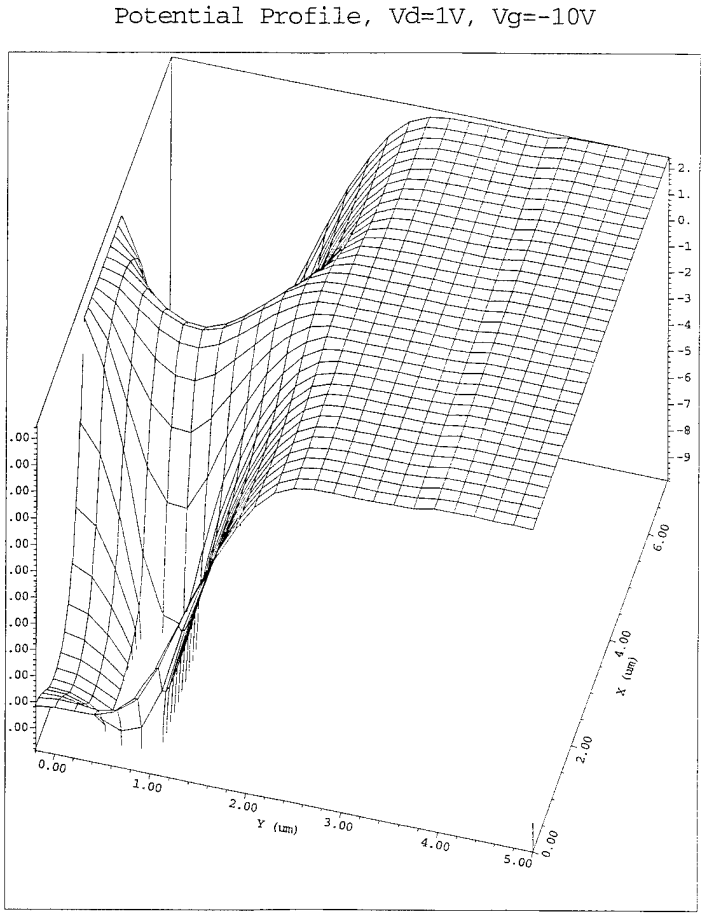
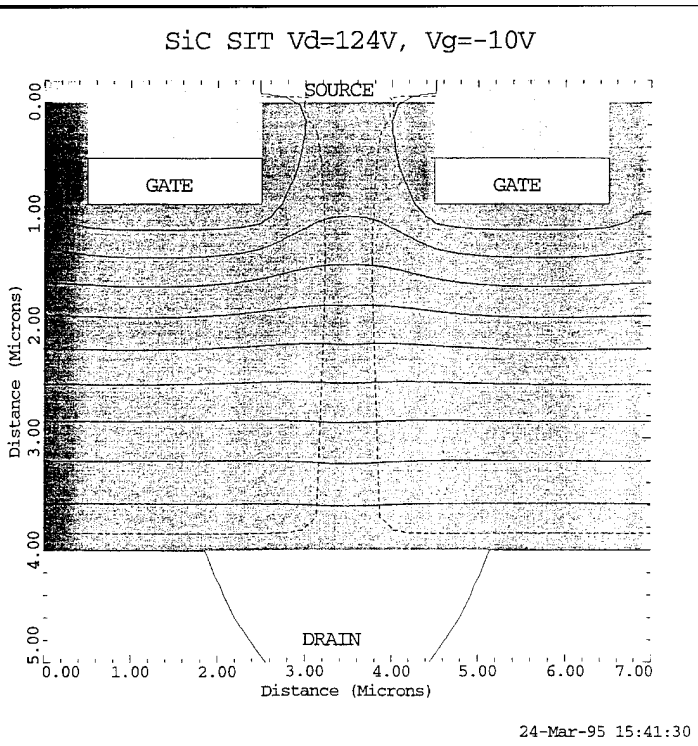


Figure 4.9 — SiC SIT model showing the device in the "off" condition. Note the potential barrier created between the two gate regions.



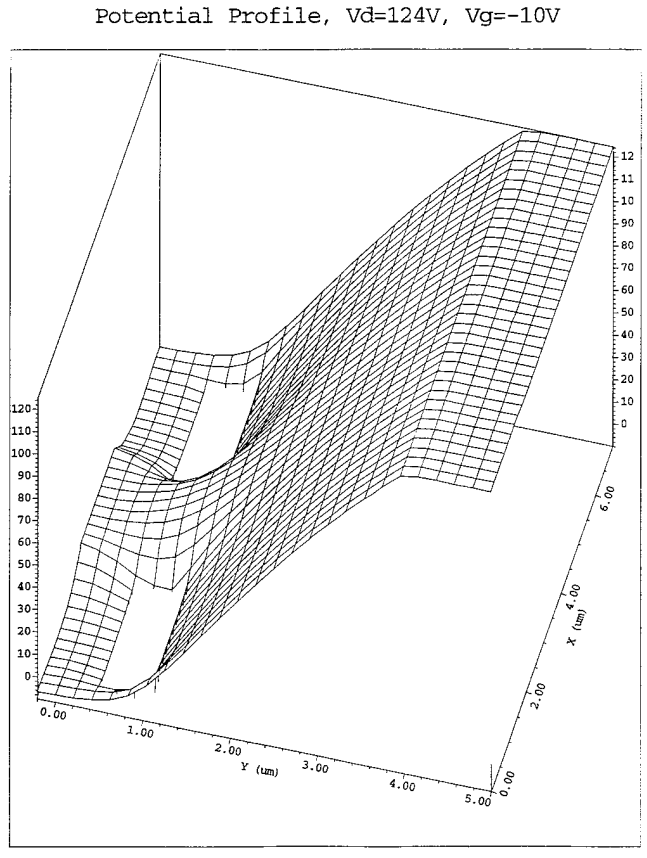


Figure 4.10 — SiC SIT model showing the device in the "on" condition. The potential barrier has been lowered permitting current flow from source to drain.

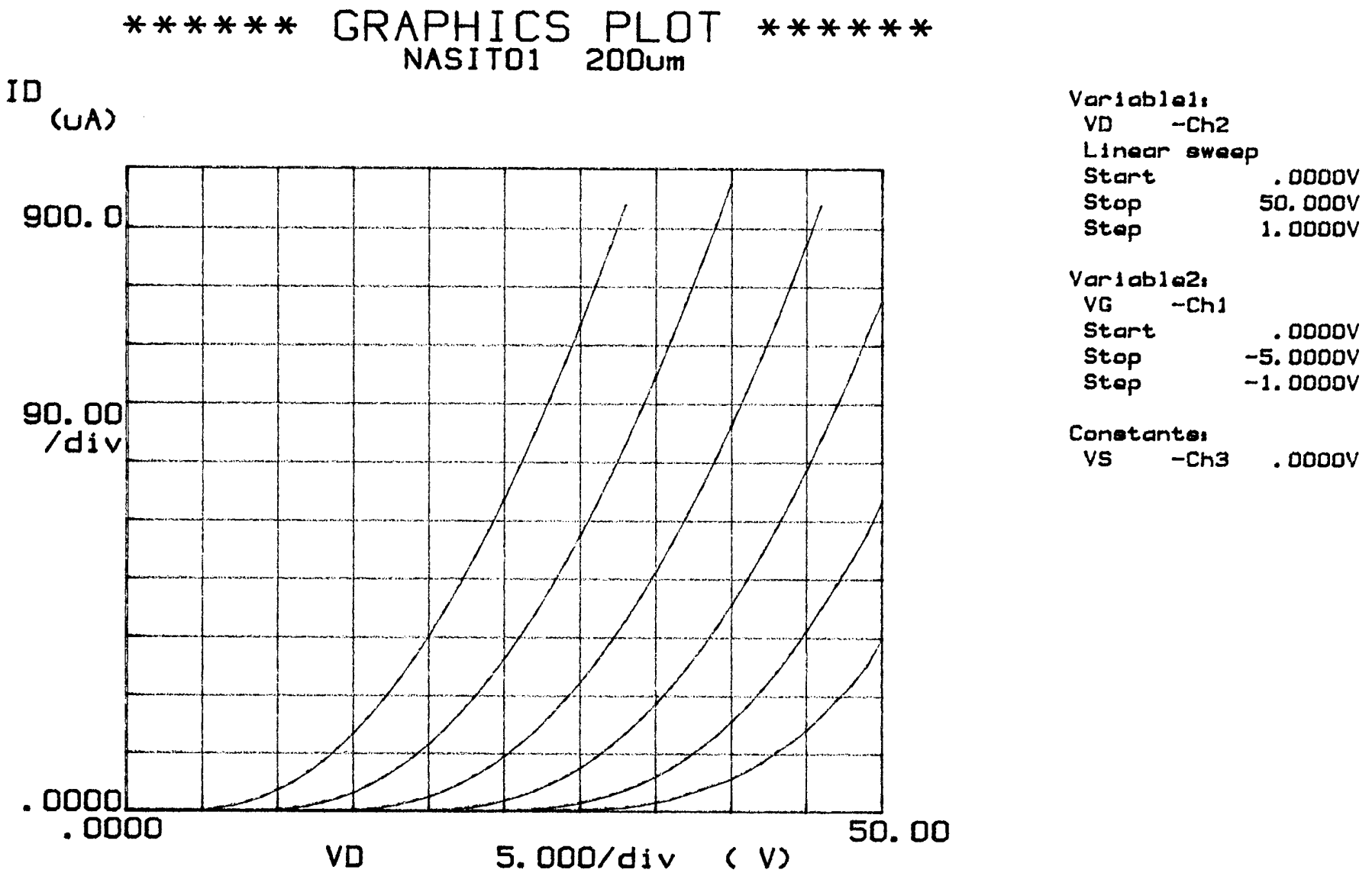


Figure 4.11 — The first SiC SIT transistor characteristics show classic triode behavior.

SiC SIT FABRICATION PROCESS

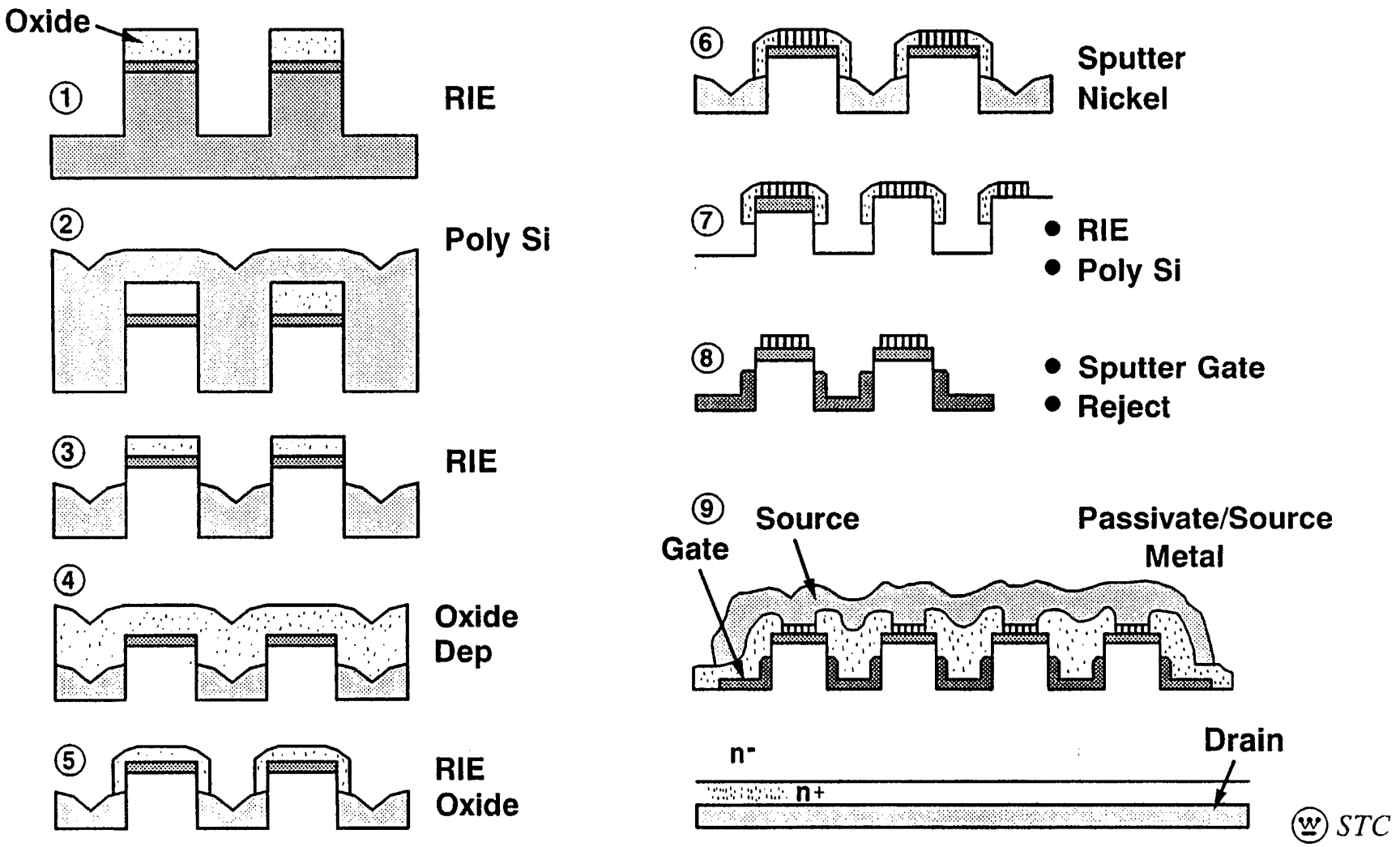


Figure 4.12 — SiC SIT fabrication process (schematic).

reveal the source contacts and gate pads. To complete the device a 2 to 3 μm thick gold layer was defined to interconnect all the SIT fingers and add source and gate bond pads on top of the field oxide. Device function was as shown in Figure 4.13, maximum channel current was 300 mA/cm, the transconductance (Gm) was 30 mS/cm and the voltage gain (μ) was 8. Monolithic SIT chips were packaged, screened for dc performance, and wirebonded in parallel, as shown in Figure 4.14. 30W of output power was developed from an eleven cm periphery SIT at 175 MHz with a power added efficiency of 60% as shown in Figure 4.15. Output power density was 3 W/cm of transistor source periphery.

Observed maximum current in 6H SiC SITs were considerably below that predicted by computer models. Reduced transistor currents adversely impact power gain and power added efficiency. The reduced current drive was identified as due to the anisotropic electron mobility in 6H SiC. Figure 4-16 shows extracted electron mobility and saturated electron velocity data measured in SIT-like samples of 6H and 4H SiC. A five-fold reduction in electron mobility along the c-axis was observed in 6H when compared to 4H. All subsequent work has therefore been directed toward the development of a 4H SiC SIT. *This completed the goals for Task 5.*

Task #6 — Second Iteration SIT Design, Fabrication, & Test

After the discovery of the improved properties of 4H SiC, efforts to provide low defect density, highly conducting n-type substrates in 4H SiC, and provide controlled CVD layers having sufficiently uniform doping profiles formed the basis of the materials work. Figure 4.17 shows a 4H-SiC n+ wafer prepared for CVD, illustrating the rapid technical progress achieved in this area. Epitaxial layers with good morphology and doping profiles similar to that shown in Figure 4.8 were then produced on 4H-SiC.

In addition to the improvements afforded by the electrical properties of 4H SiC, SIT devices were redesigned to take advantage of an improved processing

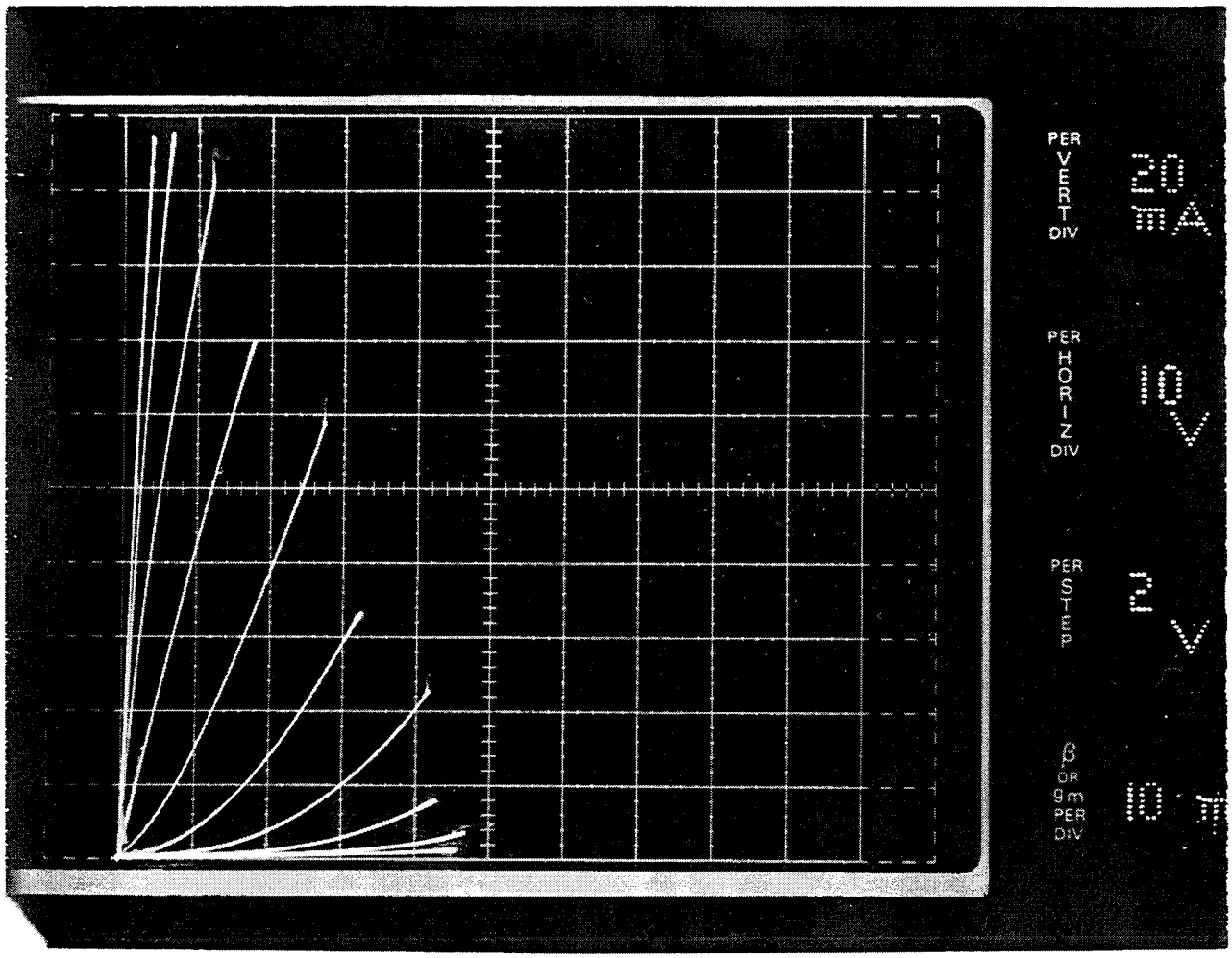


Figure 4.13 — The dc characteristic of a 3 cm source periphery SiC SIT.

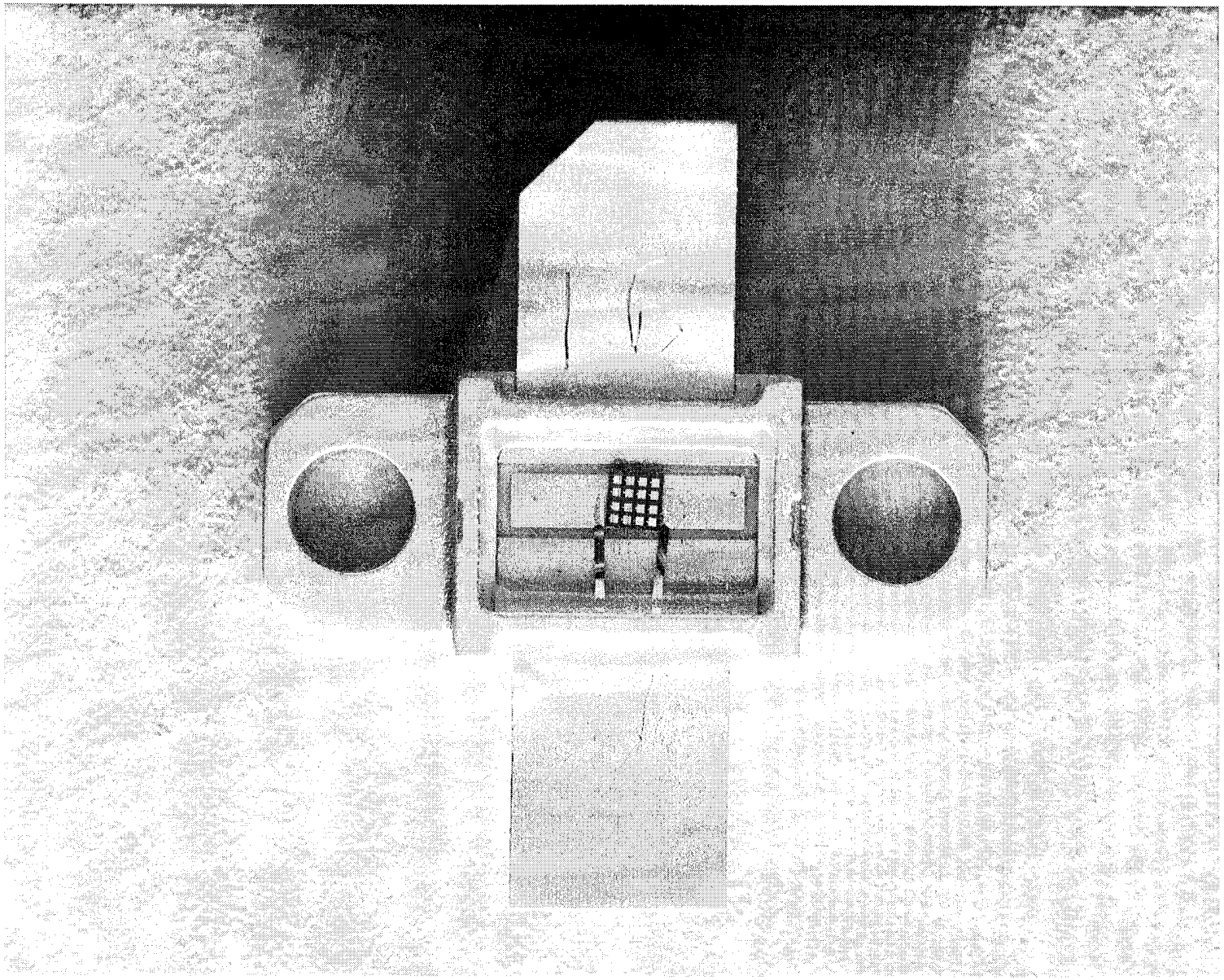


Figure 4.14 — Microwave packaging of a SiC SIT.

30W SILICON CARBIDE SIT

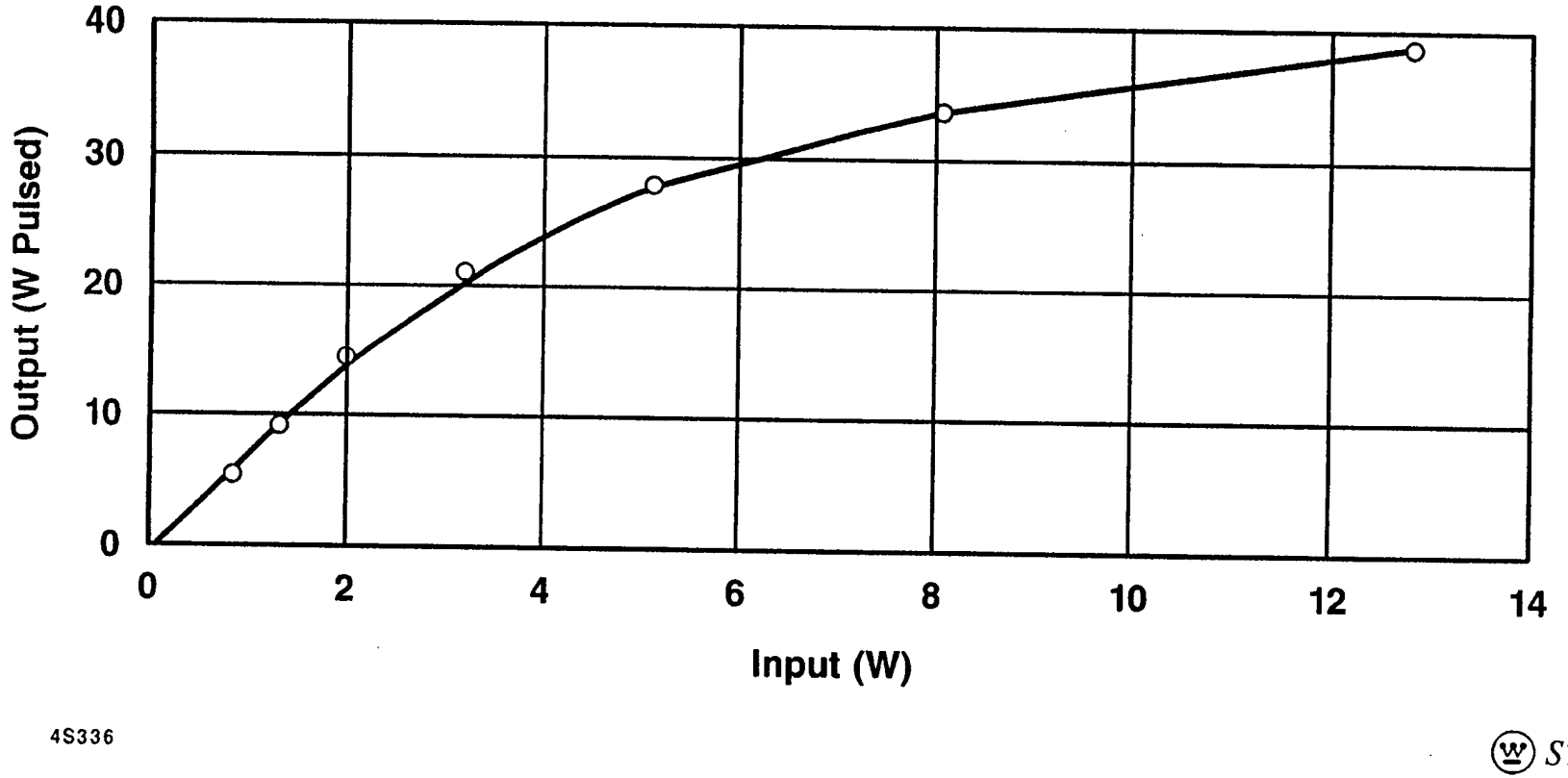


Figure 4.15 — Power performance of an 11 cm source periphery 6H SiC SIT. 30W output power obtained at 175 MHz.

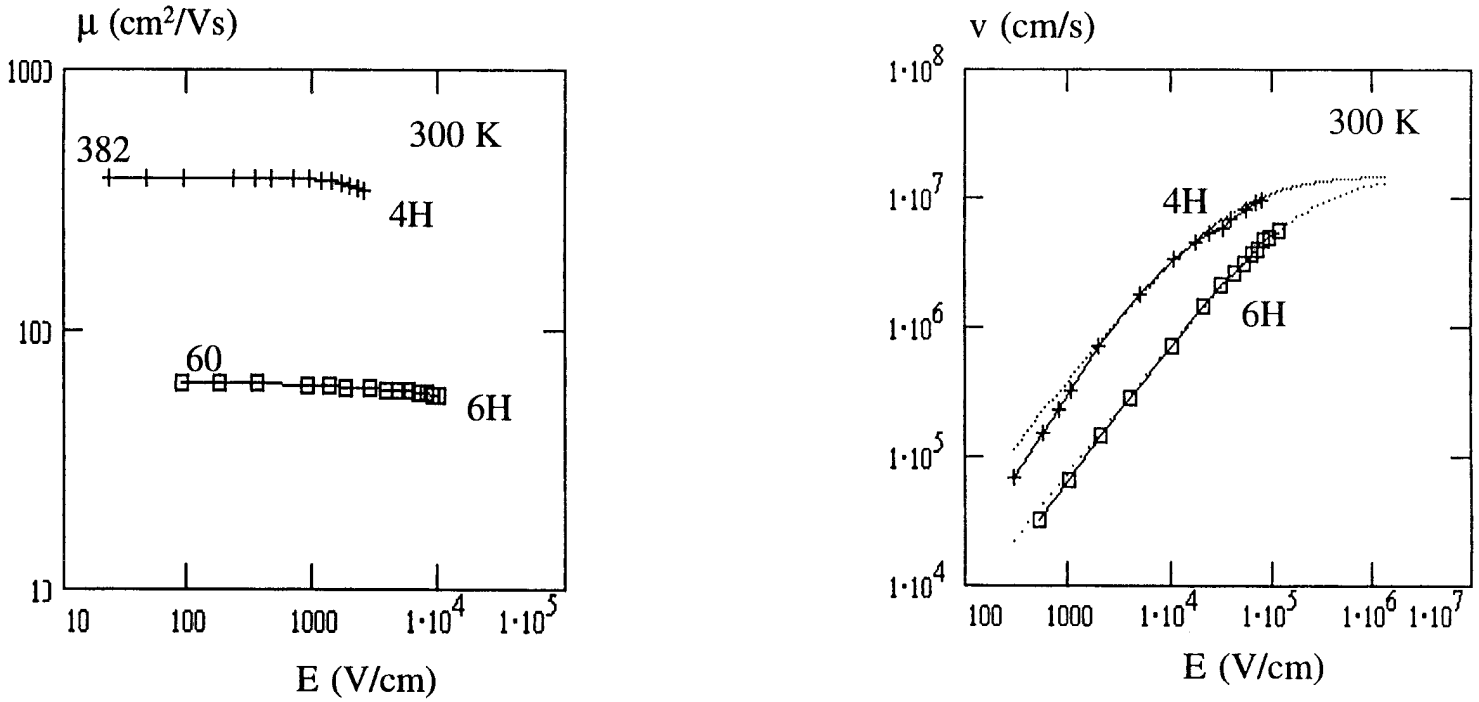


Figure 4.16 — Electron mobility and drift velocity measurements for 4H and 6H SiC SIT structures showing reduced electric mobility in 6H material.

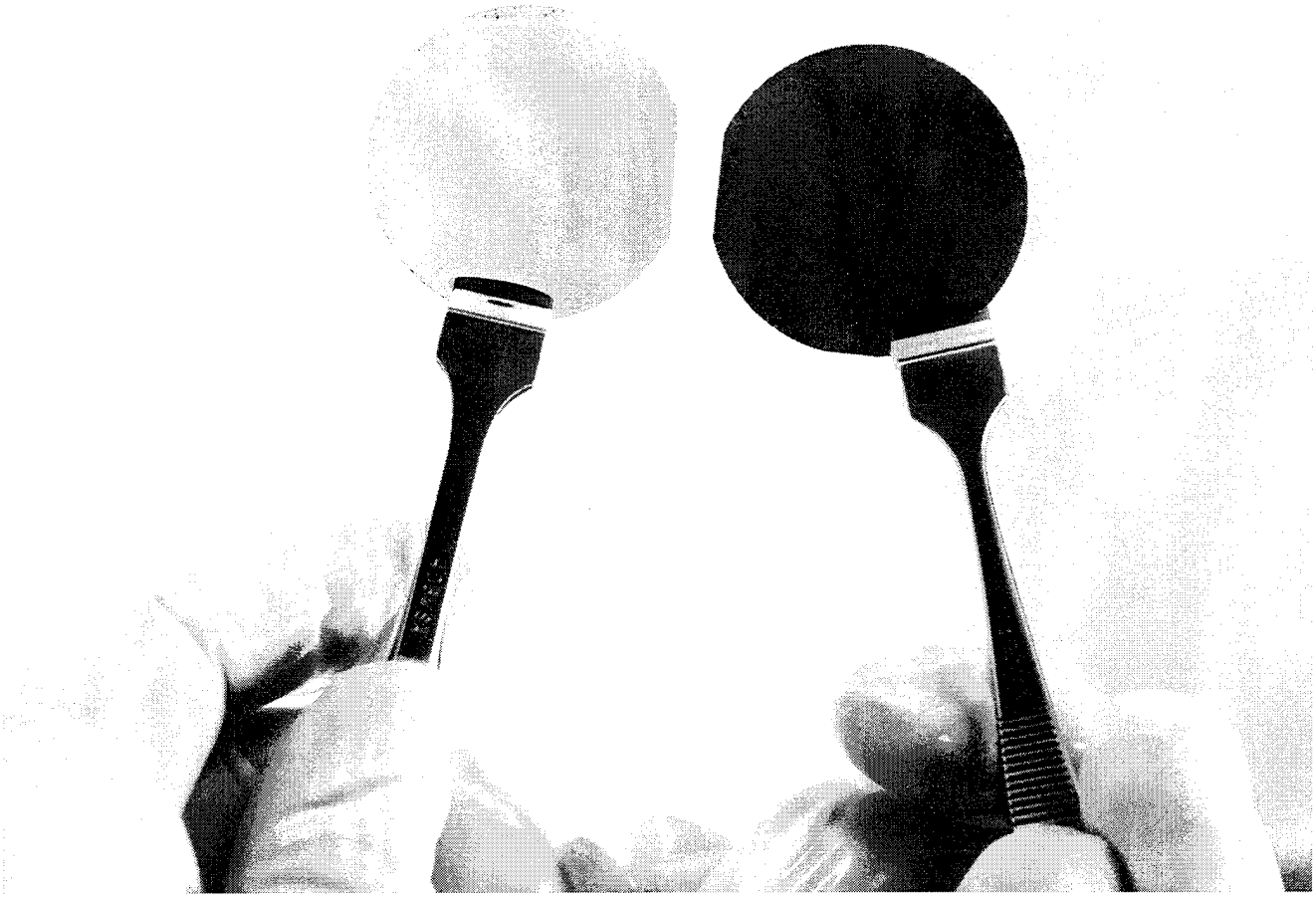


Figure 4.17 — Photograph of nitrogen-doped 4H SiC (top) and 6H (bottom) wafers for SIT fabrication.

technique that used all e-beam defined metal layers. An SEM micrograph of a completed SIT device is shown in Figure 4.18. As shown in Figure 4.19, subsequent 4H SITs showed increased drive (0.8-1A per cm) with Gm as high as 75 mS/cm. 'On wafer' RF measurements using cascade probes were used to evaluate SIT small signal performance and measure transistor s-parameters. SIT s-parameters were then fitted to a lumped element model. As shown in Fig. 4.20, the significance of this analysis is that it identifies practical reductions in SIT parasitics (e.g. gate resistance) that will raise SIT frequency response , and power performance. Packaged devices delivered 15 to 20 W/cm of device periphery with 10 dB of associated gain and 60% power added efficiency at 500 MHz. At 800 MHz the same 1 cm source periphery device delivered 11.75W output power with 42% power added efficiency and 9.7 dB of associated gain.

A subsequent fabrication run employed thermally improved SIT designs that used a finger width of 50 μm instead of the 200 micron wide fingers of the earlier design. The small signal data for these devices is shown in Figure 4.21. *Cut-off frequencies as high as 5 GHz were observed and the devices delivered 6 dB of small signal gain at 2 GHz. This performance achieves the milestone for Task 6 for the program.* Lumped element analysis shows that for this 0.25 cm source periphery device the principal improvements were in: Gm (136 mS/cm vs. 46 mS/cm) and in gate resistance (0.3 ohm/cm vs. 3.7 ohm/cm) arising from reduced contact resistance and

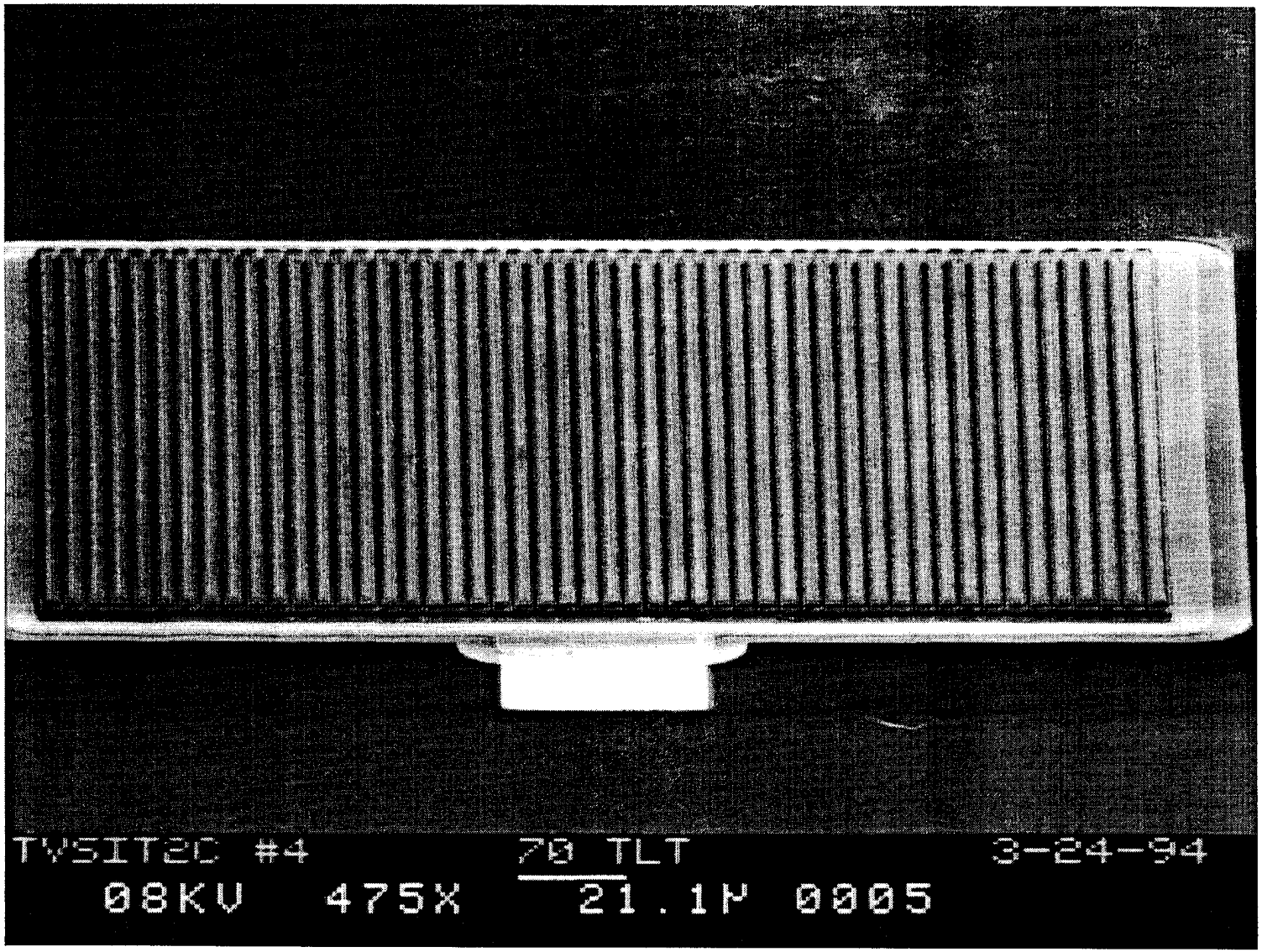


Figure 4.18 — SEM picture of completed 1 cm source periphery SIT.

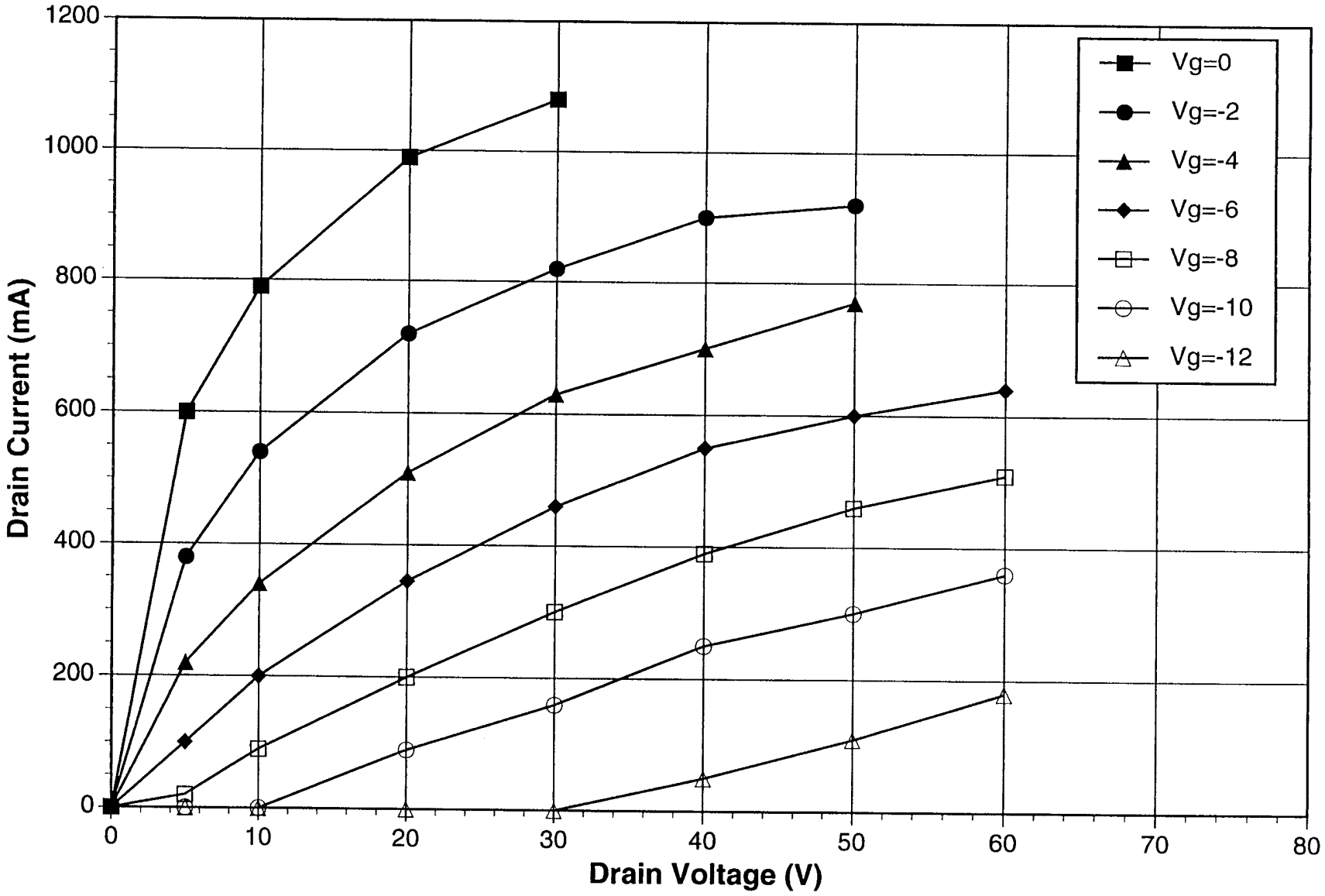


Figure 4.19 — 4H-SiC SIT dc characteristics.

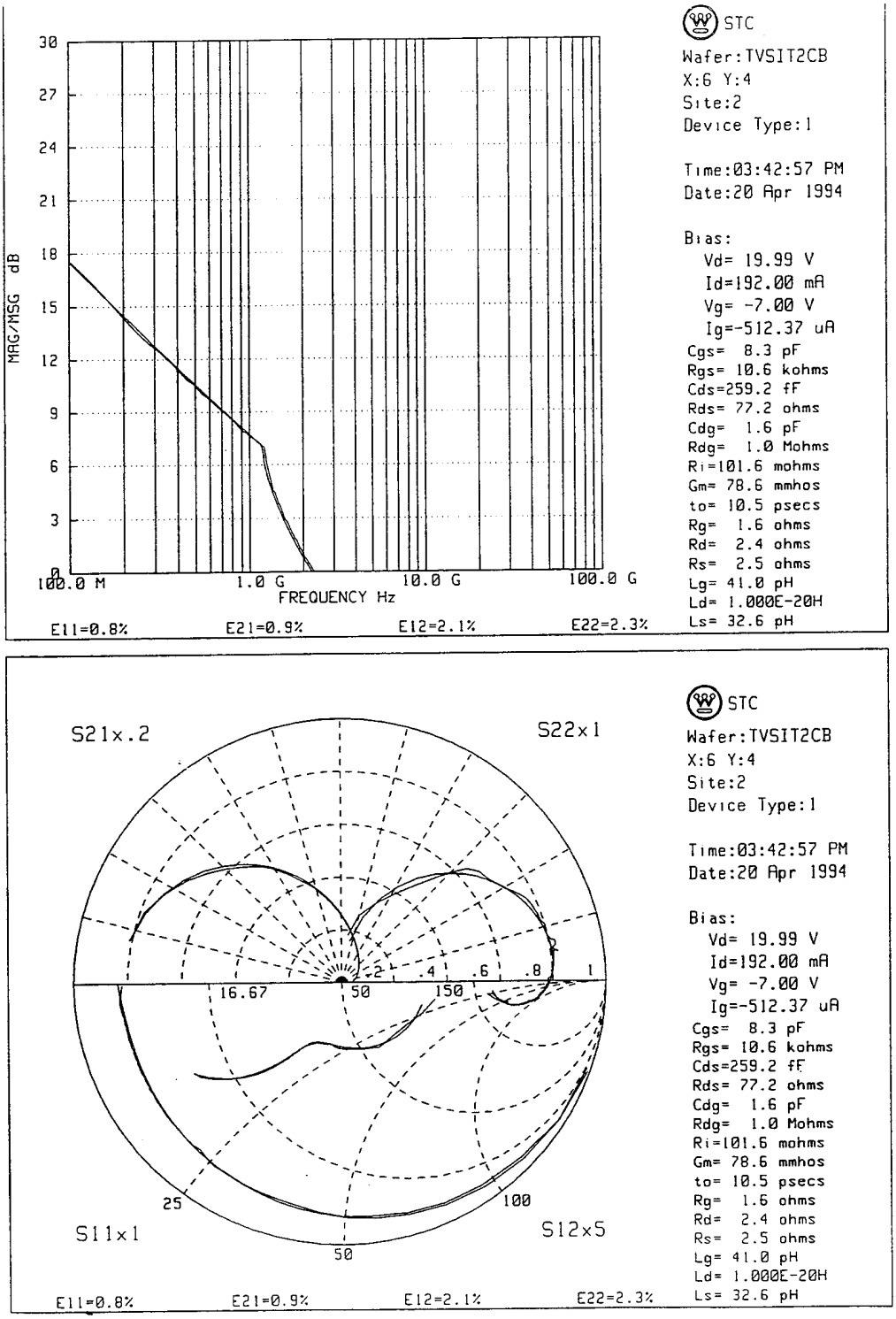


Figure 4.20 — S-parameter measurements and the extracted lumped element model of a SiC SIT.

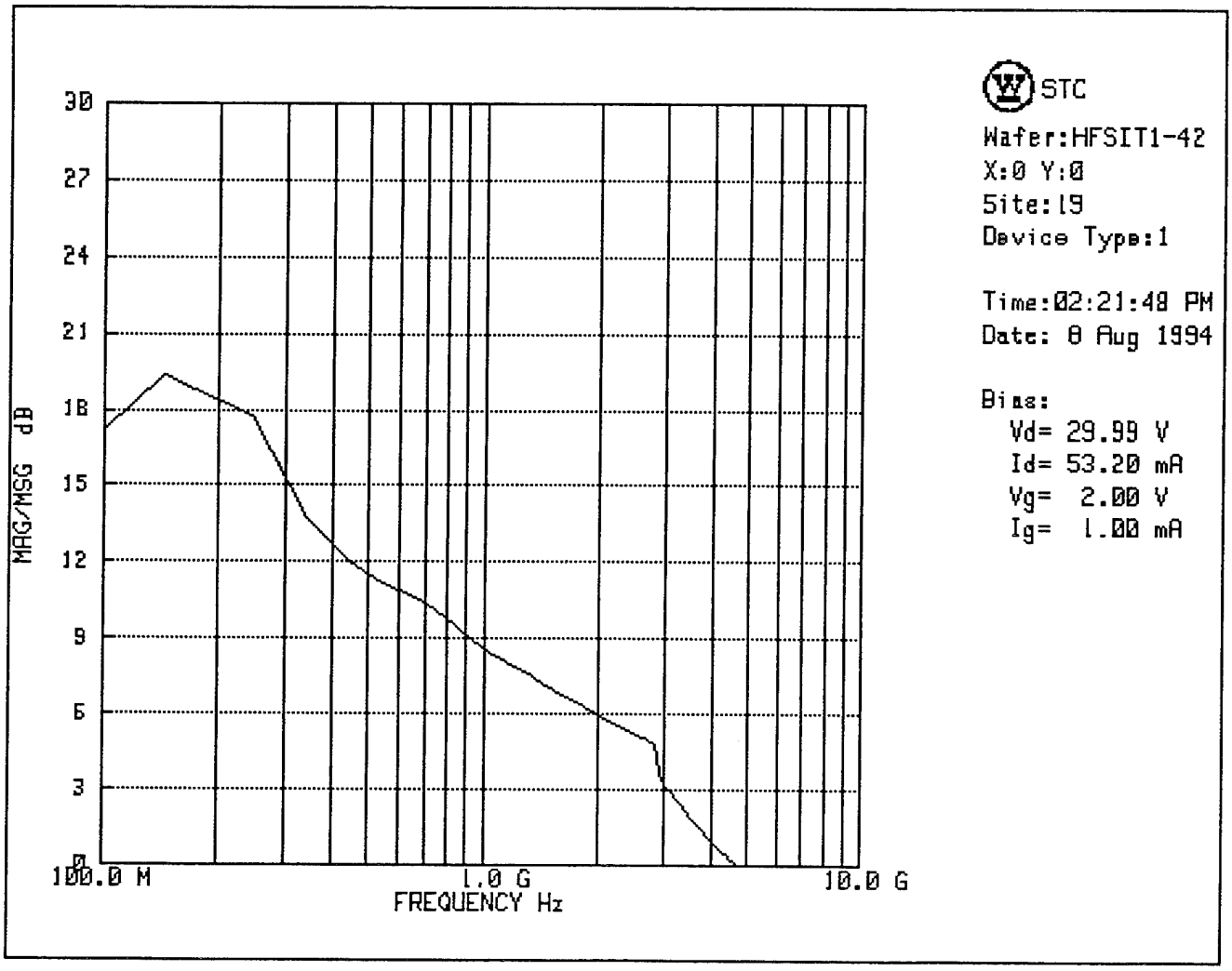


Figure 4.21 — Small signal data for devices with improved designs.

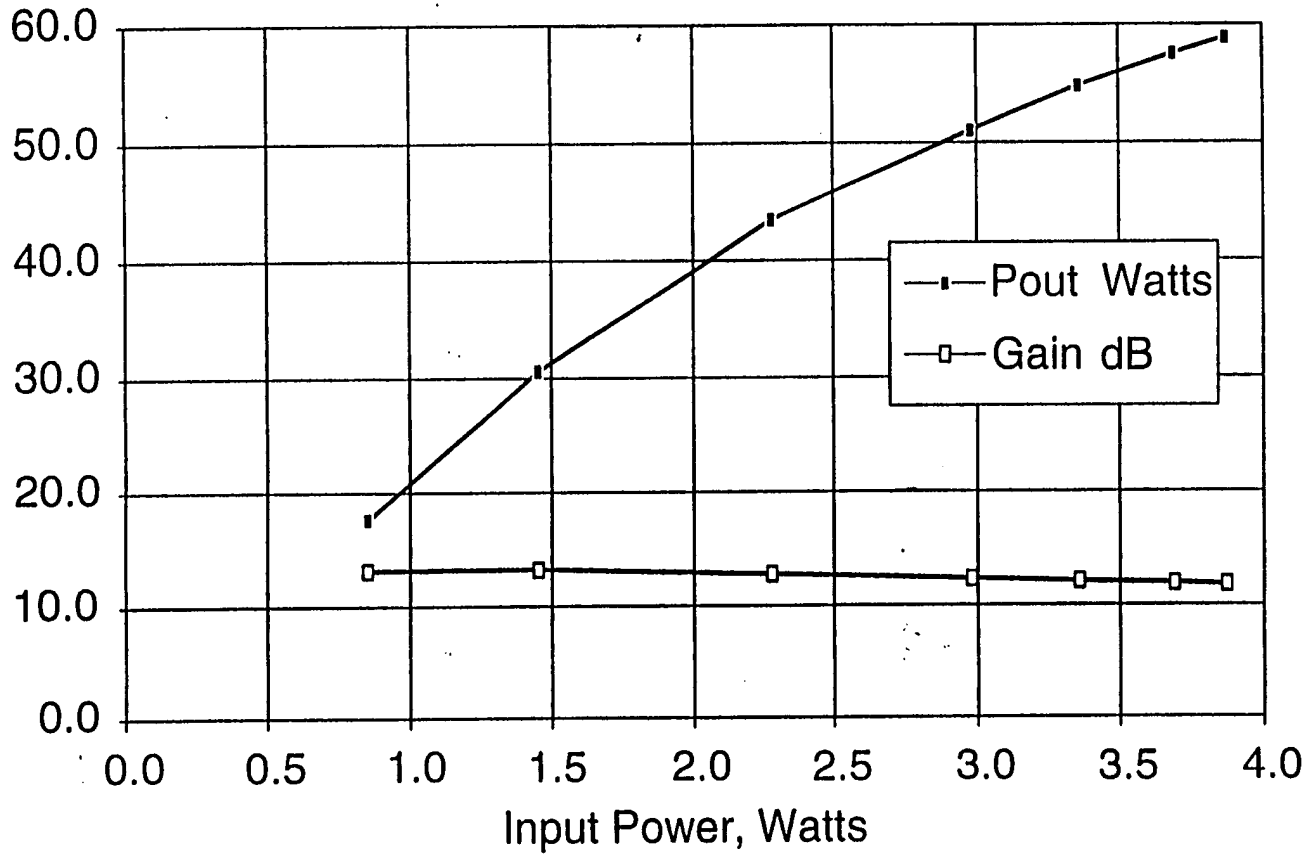


Figure 4.22 — Power performance of SiC 4.75 cm SIT @ 500 MHz.

reduced gate resistance respectively. After packaging, 4.75 cm of SIT source periphery was wire-bonded together and tested for RF power performance. At 500 MHz the device delivered 57W of output power with an associated gain of 12 dB and a power added efficiency of 43%. Power test results can be seen in Figure 4.22. Yield of dc functional 4H SiC SITs on some chips was up to 50%.

It should also be noted that significant improvement in frequency response is projected for the case of a reduced area gate that reduces gate to drain capacitance and a reduced area source that reduces gate to source capacitance. These simulations indicate that substantial power gain will be available from 4H SiC SITs at S-band.

CONCLUSIONS:

The worlds first 4H SiC SITs have shown valuable power performance up to frequencies of 1 GHz. These results include power added efficiency above 50% and power densities as high as 20W per cm of SIT source periphery. Computer de-embedding of parasitic elements from these structures confirm that substantial power at 4 GHz frequencies will be available from SiC SITs when suitably redesigned. Future work should address SIT redesign for higher frequency operation, and transistor yield improvement through the reduction of defects in SiC substrates and epitaxial layers. Adoption of practical, low cost fabrication techniques for high frequency SIT devices will also be needed for the population of the very powerful radar antennas and microwave transmitter modules of the future.

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